NVIDIA ConnectX-9 SuperNIC Firmware Release Notes v82.49.1014 (June 2026 GA Release)

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This version is not intended for GB/B customers. GB/B customers should use the designated release package to ensure full compatibility, qualification, and support alignment.

1 Release Notes Update History

Version	Date	Description
82.49.1014	June 2026	Initial release of this Release Notes version.

2 Overview

The NVIDIA® ConnectX®-9 SuperNIC™ unleashes next-generation gigascale AI with up to 800 Gb/s per port over InfiniBand and Ethernet, delivering ultra-fast, efficient connectivity that supercharges AI data centers and cloud platforms. Fully integrated with NVIDIA Spectrum-X™ Ethernet and Quantum-X800 networking, it drives up to 1.6 Tb/s of throughput to Rubin GPUs, while advanced programmable IO and intelligent congestion control maximize performance and efficiency.

2.1 Firmware Download

Please visit Firmware Downloads.

3 Firmware Compatible Products

These are the release notes for the NVIDIA® ConnectX®-9 SuperNIC firmware.

ConnectX-9 firmware supports the following speeds/protocols:

- InfiniBand - NDR, XDR
- Ethernet - 100GbE, 200GbE, 400GbE, 800GbE
- PCI Express Gen6., supporting backwards compatibility for v5.0, v4.0, v3.0, v2.0 and v1.1

> ⚠ When connecting an NVIDIA-to-NVIDIA adapter card in ETH PAM4 speeds, Auto-Neg should always be enabled.

For additional supported speeds/protocols by the ConnectX-9 ASIC, please refer to the hardware User Manual.

3.1 Supported Devices

Refer to the hardware documentation for the list of supported devices.

Driver Software, Tools and Switch Firmware

The following are the drivers' software, tools, switch/HCA firmware versions tested that you can upgrade from or downgrade to when using this firmware version:

	Supported Version
ConnectX-9 Firmware	82.49.1014 / 82.48.1000
DOCA-HOST	3.4.0 / 3.3.0 **Note:** For the list of the supported Operating Systems, please refer to the driver's Release Notes.
WinOF-2	26.4.50010 / 26.1.50000 **Note:** For the list of the supported Operating Systems, please refer to the driver's Release Notes.
MFT	4.36.0-147 / 4.35.0-159 **Note:** For the list of the supported Operating Systems, please refer to the driver's Release Notes.
FlexBoot	3.9.101
UEFI	14.42.11
NVOS	25.02.6000 onwards
Quantum-3 FW (part of NVOS)	35.2016.2080 onwards

4 Changes and New Features

To generate PLDM packages for firmware updates, users must install and use the MFT version that corresponds with the respective firmware release.

Feature/Change	Description
82.49.1014	
PCC/ZTR-RTT Congestion-Control Histogram Collection	Added support for Congestion-Control histogram collection in the PCC/ZTR-RTT algorithm. After enabling this capability, customers can read RATE and RTT histogram counters for PCC-managed flows.
Precoded Data Reception Support	Added support for receiving precoded data on the NVIDIA Rx side to ensure signal integrity performance. **Note:** To support this capability, the Tx connected to the NVIDIA Rx must transmit precoded data.
PCC TopoAware PLB (probe_metadata Behavior)	`PCC_CONFIG.probe_metadata` is now supported as a global setting that applies uniformly across all probe slots. Updates made via CREATE/MODIFY (regardless of probe_type_slot) propagate to all slots.
ZTR_RTTCC Tunable Probe Timeout	Added a new parameter to the ZTR_RTTCC algorithm to define the probe-packet timeout threshold.
PTP/PPS/SyncE over I2C DC-TCXO	Firmware now enables full timing functionality on ConnectX-9: PTP (Precision Time Protocol, IEEE 1588) time synchronization, PPS (Pulse Per Second) input/output, and SyncE (Synchronous Ethernet) frequency synchronization on platforms that use an external DC-TCXO. This is done by adding I2C-based control of the DC-TCXO so the NIC can steer/discipline its reference clock for accurate and stable timing.
Link up/Down dmesg Messages	When powering down the OSFP port, the link up/down dmesg messages were previously sent only to the primary ASIC, they are now sent to the secondary ASIC as well.
PSP Transport Packet Reformat	Added support for a new packet reformat type for PSP transport packets. This reformat removes the PSP trailer and the UDP + PSP transport headers, and updates the IP Protocol field based on the PSP next_header value.
Persistent CRDT Token	CRDT token behavior has changed and is now persistent. Previously, debug firmware was allowed only if a CRDT token was applied temporarily, meaning it was erased after reset, or if another debug firmware was already running. Once a user moved to production firmware, a new token was required to switch back to debug firmware. With the new behavior, the token is saved to flash, meaning it remains readable via MDSR even after reset. Once installed, the token allows the user to move between debug and production firmware until it is explicitly revoked using the MDSR set command.
Bug Fixes	See Bug Fixes section.

For the list of changes and bug fixes in earlier versions, see Release Notes History section.

4.1 Customer Affecting Changes

4.1.1 Changes in This Release

This section provides a list of changes that took place in the current version and break compatibility/interface, discontinue support for features and/or OS versions, etc.

Introduced in Version	Description
N/A	N/A

4.1.2 Changes Planned for Future Releases

This section provides a list of changes that will take place in a future version of the product and will break compatibility/interface, discontinue support for features and/or OS versions, etc.

Planned for Version	Description
N/A	N/A

4.1.3 Changes in Earlier Releases

This section provides a list of changes that took place throughout the past two major releases that broke compatibility/interface, discontinued support for features and/or OS versions, etc.

For an archive of all changes, please refer to the Release Notes History section.

Introduced in Version	Description
82.48.1000	**Transition to 2023 Microsoft UEFI Certificate Authority**: To align with updated Microsoft UEFI Secure Boot requirements and the upcoming end-of-life of the 2011 Certificate Authority (CA), NVIDIA is transitioning to the 2023 CA. To ensure successful loading of the Expansion ROM (ExpROM) during the UEFI Secure Boot process, system BIOS and operating system trust stores must be updated to include the 2023 CA. **Note:** When performing a firmware update of ConnectX and BlueField devices the new certificate is required for Secure Boot. To continue supporting Secure Boot, systems must be updated to recognize the "Microsoft Option ROM UEFI CA 2023."

	When using an optics module, if the required speed is lower than the module's maximum supported speed, the user must configure the desired port link width.
	Note: This configuration must be repeated after every system reboot.
	To avoid reconfiguring it manually after each reboot, configure the requested speed using the following commands:
	`mlxconfig -d <device> set PHY_RATE_MASK_OVERRIDE_P<port>=1`
	`mlxfwreset -d <device> r -y --no_mst`
	`mlxconfig -d <device> set PHY_RATE_MASK_P<port>=<PTYS.speed_mask>`
	`mlxfwreset -d <device> r -y --no_mst`
	Where `<PTYS.speed_mask>` is the speed mask defined in the PRM.

4.1.4 Discontinued Features

List of features which are supported in previous generations of hardware devices.

- InfiniBand: FDR and lower speeds

> ⚠ For inquiries regarding mitigation, please contact NVIDIA Support.

4.2 Declared Unsupported Features

The following are the unsupported features for ConnectX-9 SuperNIC in this firmware version:

- Zero Touch Tuning (ZTT)
- Hot reset
- Segment on PCIe switch
- LAG Bonding with Q-Affinity
- ISSU
- The following protocols:
    - 25 /50G NRZ
    - 800GbE
    - EDR and HDR

5 Bug Fixes in this Firmware Version

Internal Ref.	Issue
4812446 / 4917369	**Description:** Fixed an issue where CREATE_PARSE_GRAPH_NODE incorrectly applied validation intended for WA mode, in which `header_length_field_offset` is adjusted by firmware. Since ConnectX-8 and newer adapters use normal mode only, these checks were redundant and could reject valid input. Validation is now mode-specific: normal-mode rules are applied on ConnectX-8 and newer adapters, while WA-mode rules are applied on older adapters.
	Keywords: Parse graph node
	Detected in version: 82.48.1000
	Fixed in Release: 82.49.1014
4864823 / 4858750	**Description:** Fixed an issue where, when Flex Parser overwrite native arc was enabled, destroying or closing a parse graph node on a native protocol arc did not restore the native protocol parser. As a result, the native parser remained unavailable on the device until a reset or another recovery action was performed. Native protocol parsing is now restored as expected when the parse graph node is closed or destroyed. Native parsers are disabled only while the Flex Parser graph owns the arc.
	Keywords: Flex Parser
	Detected in version: 82.48.1000
	Fixed in Release: 82.49.1014
4895996 / 4965646 / NVBug 5919232	**Description:** Fixed an issue where the MCU sometimes NACKed I2C MCTP transactions. A retry mechanism has been implemented for NACK cases.
	Keywords: MCU, NACK
	Detected in version: 82.48.1000
	Fixed in Release: 82.49.1014
4902573	**Description:** Fixed an issue where executing CancelComponentUpdate during the firmware burn FSM_RET_BUSY window caused firmware to return error 0x84 (Invalid state) and left WP disabled.
	Keywords: PLDM update, WP
	Detected in version: 82.48.1000
	Fixed in Release: 82.49.1014
4964566 / 4957757	**Description:** Fixed a DEAD IRISC assert that could occur during TLV NV_DATA flash access by suspending the watchdog while waiting for flash IPC (until timeout), preventing the assert on TLV access.
	Keywords: DEAD IRISC assert
	Detected in version: 82.48.1000

Internal Ref.	Issue
	Fixed in Release: 82.49.1014
4835832	**Description:** In rare cases, certain module types may experience link-up failures.
	Keywords: Cables
	Detected in version: 82.48.1000
	Fixed in Release: 82.49.1014
4871267 / 4871254	**Description:** Fixed an issue where ICM_RES_HW_DMFS_ENCAP_H_FW was allocated per GVMI, preventing some RTTs from using it.
	Keywords: GVMI, RTT
	Detected in version: 82.48.1000
	Fixed in Release: 82.49.1014
4860860	**Description:** Fixed an issue where queue pairs (QPs) created during a PCC process transition could miss congestion-control (CC) information, preventing them from being fully managed.
	Keywords: DOCA, PCC, QP, Congestion Control
	Detected in version: 82.48.1000
	Fixed in Release: 82.49.1014
4789601 / 4850200 / NVBug 5736447	**Description:** Fixed an issue where RDMA traffic could stall in large-scale deployments for certain source IP and UDP source-port combinations when DOCA PCC was active and no congestion-control algorithm was configured in algorithm slot 0.
	Keywords: RDMA, DOCA PCC, Congestion Control Algorithm
	Detected in version: 82.48.1000
	Fixed in Release: 82.49.1014
4796182	**Description:** Fixed an issue where the live migration target did not receive a port state change event on the resume VHCA command. The target now generates this event so software that depends on port state is notified of any changes.
	Keywords: Live migration
	Detected in version: 82.48.1000
	Fixed in Release: 82.49.1014
4867472 / 4847702 / 4642994 / 4859742	**Description:** Fixed an issue during hitless upgrade where, after the SACK generation/handler fence, firmware could mark the old port configuration ID as invalid. If SACK causes were still active, a race could cause SACK ISRs to stop unexpectedly. The fix is to always return BUSY while handover is active.
	Keywords: Hitless upgrade

Internal Ref.	Issue
	Detected in version: 82.48.1000
	Fixed in Release: 82.49.1014
4873533 / 4947034	**Description:** Fixed an issue where, when using multiplane ZTRCC congestion control with multiple flows, the RTT timeout counter in the PPCC register could increase even when the network was not congested.
	Keywords: Congestion control, multiplane, SPCX CC, RTT, PPCC
	Detected in version: 82.48.1000
	Fixed in Release: 82.49.1014
4843342 / 4970550	**Description:** Fixed an issue where one-to-one RoCE traffic using a single QP might not achieve line rate on some platforms when using the default ROCE_CC_COMPATIBILITY_MODE setting in mlxconfig.
	Keywords: Congestion control, PCC, ROCE_CC_COMPATIBILITY_MODE
	Detected in version: 82.48.1000
	Fixed in Release: 82.49.1014

6 Known Issues

ConnectX-9 has the same feature set and limitations as the ConnectX-8 SuperNIC. For the list of ConnectX-8 known issues, refer to: https://docs.nvidia.com/networking/software/adapter-firmware/index.html#connectx-8.

The limitations listed below apply to ConnectX-9 only.

Internal Ref.	Issue
4721472	**Description:** Direct Memory Access (DMA) protection is not supported in the ipxe.efi driver.
	Workaround: N/A
	Keywords: DMA
	Detected in version: 82.49.1014
4835832	**Description:** In rare cases, certain module types may experience link-up failures.

	Workaround: Configure the requested speed using the following commands:
	`mlxconfig -d <device> set PHY_RATE_MASK_OVERRIDE_P<port>=1`
	`mlxfwreset -d <device> r -y --no_mst`
	`mlxconfig -d <device> set PHY_RATE_MASK_P<port>=<PTYS.speed_mask> (speed mask is defined in PRM)`
	`mlxfwreset -d <device> r -y --no_mst`

	Keywords: Cables
	Detected in version: 82.48.1000
4809493 / 4804815 / 4884845	**Description:** Running lane margin tests may disrupt traffic, cause connection drops, or degrade performance.
	Workaround: 1. Disable the drivers before starting the Lane Margin test. 2. Set an error threshold of 2. 3. If the connection drops or performance degrades, re-run the process.
	Keywords: Lane Margin
	Detected in version: 82.48.1000
4806964 / 4829338 / 4843305 / 4857738	**Description:** When bringing up 800G_8x on ConnectX-9 with Spectrum-4 switch systems, switch firmware version xx.201.3916-020 or later is required; earlier versions may fail to link up at 800G_8x.
	Workaround: N/A
	Keywords: Linkup, cables, Spectrum-4, 800G_8x
	Detected in version: 82.48.1000

7 PreBoot Drivers (FlexBoot/UEFI)

7.1 FlexBoot Changes and New Features

For further information, please refer to the FlexBoot Release Notes.

7.2 UEFI Changes and Major New Features

For further information, please refer to the UEFI Release Notes.

8 Validated and Supported Cables and Switches

8.1 Validated and Supported Cables and Modules

8.1.1 Cables Lifecycle Legend

Lifecycle Phase	Definition
EOL	End of Life
LTB	Last Time Buy
HVM	GA level
MP	GA level
P-Rel	GA level
Preliminary	Engineering Sample
Prototype	Engineering Sample

8.1.2 XDR / 800GbE / 1600GbE Cables

IB Data Rate	Eth Data Rate	NVIDIA SKU	Marketing Description	LifeCycle Phase
NA	800GE	980-9IAY1-00XM00	NVIDIA single port transceiver, DR4, 800Gbps, OSFP, MPO(APC), 1310nm SMF, up to 500m, RHS, FRO, Gen2, Ethernet Only	Early BOM
NA	1600GE	980-9IAU1-00XM00	NVIDIA twin port transceiver, 2xDR4, 1600Gbps, OSFP, 2xMPO(APC), 1310nm SMF, up to 500m, RHS, FRO, Gen2, Ethernet Only	Early BOM
XDR	1600GE	980-9IAM1-00X001	NVIDIA Active copper cable, 1600Gbps to 1600Gbps, OSFP, 1.1m, RHS to RHS, NIC to NIC	P-Rel
XDR	1600GE	980-9IAO5-00X001	NVIDIA Active copper splitter cable, 1600Gb/s to 2x800Gb/s, OSFP to 2xOSFP, 1m, IHS to RHS	P-Rel
XDR	1600GE	980-9IAO5-00X002	NVIDIA Active copper splitter cable, 1600Gb/s to 2x800Gb/s, OSFP to 2xOSFP, 2m, IHS to RHS	P-Rel
XDR	1600GE	980-9IAO5-00X01A	NVIDIA Active copper splitter cable, 1600Gb/s to 2x800Gb/s, OSFP to 2xOSFP, 1.5m, IHS to RHS	P-Rel
XDR	NA	980-9IAT0-00XM00	NVIDIA single port transceiver, 800Gbps,OSFP DR4, MPO,APC 1310nm SMF, up to 500m, RHS	P-Rel
XDR	NA	980-9IAU0-00XM00	NVIDIA twin port transceiver, 2xDR4, 1600Gbps, OSFP, 2xMPO(APC), 1310nm SMF, up to 500m, RHS, FRO, Gen2, XDR Only	Early BOM
XDR	NA	980-9IAY0-00XM00	NVIDIA single port transceiver, DR4, 800Gbps, OSFP, MPO(APC), 1310nm SMF, up to 500m, RHS, FRO, Gen2, XDR Only	Early BOM

8.1.3 NDR / 400GbE / 800GbE Cables

IB Data Rate	Eth Data Rate	NVIDIA SKU	Legacy P/N	Marketing Description	LifeCycle Phase
NDR	NA	980-9I302-00NM00	MMS4X00-NM-HGX	NVIDIA twin port transceiver, 800Gbps,2xNDR, OSFP, 2xMPO12 APC, 1310nm SMF, up to 500m, flat top - For HGX Rubin NVL8	P-Rel
NDR	NA	980-9I600-00N003	MCA4J80-N003-FLT	Active copper cable, IB twin port NDR, up to 800Gb/s, OSFP, 3m, flat top	MP
NDR	NA	980-9I601-00N003	MCA4J80-N003-FTF	NVIDIA Active copper cable, IB twin port NDR, up to 800Gb/s, OSFP, 3m, flat to finned	MP
NDR	NA	980-9IA0G-00N001	MCP4Y10-N001-FLT	NVIDIA Passive Copper cable, IB twin port NDR, up to 800Gb/s, OSFP, 1m, flat top	MP
NDR	NA	980-9IA0J-00N002	MCP4Y10-N002-FLT	NVIDIA passive Copper cable, IB twin port NDR, up to 800Gb/s, OSFP, 2m, flat top	MP
NDR	NA	980-9IA0L-00N00A	MCP4Y10-N00A-FLT	NVIDIA Passive Copper cable, IB twin port NDR, up to 800Gb/s, OSFP, 0.5m, flat top	MP
NDR	NA	980-9IA0R-00N01A	MCP4Y10-N01A-FLT	NVIDIA passive Copper cable, IB twin port NDR, up to 800Gb/s, OSFP, 1.5m, flat top	MP
NDR	NA	980-9I432-00N001	MCP7Y00-N001	NVIDIA passive copper splitter cable, IB twin port NDR 800Gb/s to 2x400Gb/s, OSFP to 2xOSFP,1m	P-Rel
NDR	NA	980-9I433-00N001	MCP7Y00-N001-FLT	NVIDIA passive copper splitter cable, IB twin port NDR 800Gb/s to 2x400Gb/s, OSFP to 2xOSFP,1m, flat top	P-Rel
NDR	NA	980-9I924-00N002	MCP7Y00-N002	NVIDIA passive copper splitter cable, IB twin port NDR 800Gb/s to 2x400Gb/s, OSFP to 2xOSFP, 2m	P-Rel
NDR	NA	980-9I925-00N002	MCP7Y00-N002-FLT	NVIDIA passive copper splitter cable, IB twin port NDR 800Gb/s to 2x400Gb/s, OSFP to 2xOSFP, 2m, flat top	P-Rel
NDR	NA	980-9I92N-00N003	MCP7Y00-N003	NVIDIA passive copper splitter cable, IB twin port NDR 800Gb/s to 2x400Gb/s, OSFP to 2xOSFP, 3m	P-Rel
NDR	800GE	980-9I75E-00N001	MCP7Y50-N001	NVIDIA passive copper splitter cable, 800(2x400)Gbps to 4x200Gbps, OSFP to 4xOSFP, 1m, fin to flat	P-Rel
NDR	800GE	980-9I75F-00N001	MCP7Y50-N001-FLT	NVIDIA passive copper splitter cable, 800(2x400)Gbps to 4x200Gbps, OSFP to 4xOSFP, 1m, flat to flat	P-Rel
NDR	800GE	980-9I46G-00N002	MCP7Y50-N002	NVIDIA passive copper splitter cable, 800(2x400)Gbps to 4x200Gbps, OSFP to 4xOSFP, 2m, fin to flat	P-Rel
NDR	800GE	980-9I46H-00N002	MCP7Y50-N002-FLT	NVIDIA passive copper splitter cable, 800(2x400)Gbps to 4x200Gbps, OSFP to 4xOSFP, 2m, flat to flat	P-Rel
NDR	800GE	980-9I46T-00N003	MCP7Y50-N003	NVIDIA passive copper splitter cable, 800(2x400)Gbps to 4x200Gbps, OSFP to 4xOSFP, 3m, fin to flat	P-Rel
NDR	400GE	980-9I693-00NS00	MMA1Z00-NS400	NVIDIA single port transceiver, 400Gbps, QSFP112, MPO12 APC, 850nm MMF, up to 50m, flat top	P-Rel
NA	400GE	980-9I693-F4NS00	MMA1Z00-NS400-T	SINGLE PORT TRANSCEIVER, 400GBPS,400GbE, QSFP112, MPO12 APC, 850NM MMF, UP TO 50M, FLAT TOP	P-Rel

IB Data Rate	Eth Data Rate	NVIDIA SKU	Legacy P/N	Marketing Description	LifeCycle Phase
NDR	800GE	980-9I51A-00NS00	MMA4Z00-NS-FLT	NVIDIA twin port transceiver, 800(2x400)Gbps, OSFP, 2xMPO12 APC, 850nm MMF, up to 50m, flat top	MP
NDR	400GE	980-9I51S-00NS00	MMA4Z00-NS400	NVIDIA single port transceiver, 400Gbps, OSFP, MPO12 APC, 850nm MMF, up to 50m, flat top	MP
NA	400GE	980-9I51S-F4NS00	MMA4Z00-NS400-T	SINGLE PORT TRANSCEIVER, 400GBPS,400GbE, OSFP, MPO12 APC, 850NM MMF, UP TO 50M, FLAT TOP	P-Rel
NDR	NA	980-9I068-00NM00	MMS1X00-NS400	NVIDIA single port transceiver, 400Gbps, NDR, QSFP112, MPO, 1310nm SMF, up to 500m, flat top	P-Rel
NDR	NA	980-9I301-00NM00	MMS4X00-NM-FLT	NVIDIA twin port transceiver, 800Gbps,2xNDR, OSFP, 2xMPO12 APC, 1310nm SMF, up to 500m, flat top	P-Rel
NDR	400GE	980-9I31N-00NM00	MMS4X00-NS400	NVIDIA single port transceiver, 400Gbps, OSFP, MPO12 APC, 1310nm SMF, up to 100m, flat top	MP

8.2 Validated and Supported Optical Fibers Cables

MFP7E	x0-	Nxxx
NVIDIA passive fiber cable, MPO12 APC	**Fiber Type** 10 = MMF 20 = **1:2** splitter MMF 30 = SMF 40 = **1:2** splitter SMF	**Fiber Length** MMF: 3, 5, 7, 10, 15, 20, 30, 35, 40, 50m SMF: 3, 5, 7, 10, 15, 20, 30, 40, 50, 60, 70

8.3 Tested Switches

8.3.1 XDR / 800GbE Switches

Speed	NVIDIA SKU	Legacy OPN	Description	LifeCycle Phase
XDR	920-9B34F-00RX-FS0	Q3200-RA	Quantum-3 based Two-Adjoining XDR InfiniBand Switches, Q3200-RA, 2U, with 36 XDR Ports over 18 OSFP cages per Switch, 4 Power Supplies (Power Cords Not Included), Standard Depth, Managed, C2P Airflow, Rail Kit	P-Rel
XDR	920-9B36F-00RX-8S0	Q3400-RA	NVIDIA Quantum-3 based XDR InfiniBand Switch, Q3400-RA, 4U, 144 XDR Ports over 72 OSFP Cages, 8 Power Supplies (Power Cords Not Included), Standard Depth, Managed, C2P Airflow, Rail Kit	P-Rel
800 GbE	920-9N42F-00RI-7C0	SN5600	NVIDIA Spectrum-4 based 800GbE 2U Open Ethernet switch with Cumulus Linux Authentication, 64 OSFP ports and 1 SFP28 port, 2 power supplies (3KW, AC), x86 CPU, Secure-boot, standard depth, C2P airflow, Tool-less Rail Kit	LTB

Speed	NVIDIA SKU	Legacy OPN	Description	LifeCycle Phase
800 GbE	920-9N42F-00RI-3C1	SN5610	Nvidia Spectrum-4 based 800GbE 2U Open Ethernet switch with Cumulus Linux Authentication, 64 OSFP ports and 2 SFP28 ports, 4 AC PSUs, Secure-boot, standard depth, Connector-to-Power Airflow, Tool-less Rail Kit	P-Rel
800 GbE	920-9N52F-00RB-YY1	SN5640	NVIDIA IPN Spectrum-5 based 400GbE 2U Open Ethernet switch with ONIE Authentication, 64 OSFP and 2 SFP28 ports, 512 MACs, 4 AC Power-Supplies, AMD CPU, Non-secured, Connector-to-Power Airflow	Pre-Production

9 Release Notes History

9.1 Changes and New Feature History

Feature/Change	Description
82.48.1000	
General	This is the initial firmware release for the NVIDIA® ConnectX®-9 SuperNIC. ConnectX-9 provides the same feature set as the ConnectX-8 adapter card. For a complete list of ConnectX-8 firmware features, refer to the ConnectX-8 Firmware Release Notes. The features described below are new and are provided in addition to the existing ConnectX-8 feature set.
Lane Margin Test (LMT)	Lane Margin Test (LMT) is a PCIe diagnostic tool that performs controlled per-lane margining in the voltage and timing domains to evaluate link robustness. It helps identify weak or unstable lanes and supports signal-integrity validation, platform bring-up, and long-term reliability analysis. **Notes:** • NVIDIA recommends setting the error threshold to **2**. LMT is a destructive test, link drops or performance degradation may occur; if this happens, rerun the test. • NVIDIA also recommends disabling drivers before starting the Lane Margin Test.
T10 Data Integrity (DIF)	This capability provides block-level data protection by appending a Data Integrity Field (DIF) to each block, including checksums and metadata. The firmware automatically verifies these fields during reads, writes, and data transfers, helping to detect and prevent data corruption, ensure end-to-end data integrity, and increase reliability for critical storage workloads. By enabling T10 DIF, systems can achieve more robust data protection, reducing the risk of silent errors and improving overall storage confidence.
Cyclic Redundancy Check (CRC)	CRC provides a fast and reliable method to detect data corruption by generating a checksum for each block of data. The firmware automatically verifies CRC values during reads, writes, and transfers, helping to detect and prevent silent data errors, ensure end-to-end data integrity, and increase overall system reliability. By leveraging CRC, storage systems can maintain high confidence in critical workloads and minimize the risk of data loss.
Transport Layer Security (TLS) Handshake	The TLS handshake establishes a secure communication session by authenticating endpoints, negotiating cryptographic algorithms, and securely exchanging encryption keys before data transfer begins. This process ensures confidentiality of data in transit, protection against tampering and man-in-the-middle attacks, and trusted identity verification, enabling secure and reliable communication for sensitive and high-value workloads.
NVMe over TCP Acceleration	This capability offloads and accelerates NVMe/TCP data path processing to hardware, reducing CPU overhead and latency while increasing throughput. By streamlining NVMe command processing and TCP handling, it enables higher IOPS, lower and more predictable latency, and improved host CPU efficiency, making it ideal for scalable, high-performance, and cloud-based storage deployments.

Feature/Change	Description
82.48.1000	
DPA Process Limit Update	The system-wide limit for DPA processes has been reduced to **30**. This total includes both user processes across all GVMIs and internal ProgCC processes. The `max_dpa_processes` value reported to the user is calculated as: `max_dpa_processes=30-number_of_progcc_processes`
Host Rate Limiting Support Above 255 Gbps	Host rate limiting has been extended to support bandwidth values above 255 Gbps. To remove the previous cap, a new `max_bw_value_msb` field was added to `est_global`, providing additional MSB bits to represent higher bandwidth values. With this enhancement, firmware and host tooling can correctly configure and report rate limits beyond 255 Gbps on high-speed links.
PLDM PDR Repository Change Event Support	PLDM now supports the PDR Repository Change event type, enabling notification to the BMC when PDRs change. With this flow, the BMC can detect cable insertion/removal events. Refer to DSP0248 for details.
BMC Write-Protection Check on Firmware Update Failure	Added a validation step during firmware updates to detect whether the BMC is asserting write protection, helping diagnose and prevent update failures.
CMB SysRAM Window Partitioning for PSC Isolation	CMB configuration enforces secure access to System RAM (SysRAM) by defining memory windows and partitions that isolate the Platform Security Controller (PSC) from other system components.
Physical Access Monitor and Protection	The Physical Monitor feature helps protect the platform against threats from attackers with physical access to the system. It monitors for physical-access events and enforces safeguards that prevent or restrict sensitive operations, reducing the risk of exposing secure information or compromising security-critical functionality.
Parallel Save/Load Support for VF Migration	Added support for running save and load operations in parallel, enabling multiple contexts (e.g., multiple VFs) to be checkpointed and restored concurrently instead of serially. This reduces overall migration time and improves scalability in environments that need to migrate or recover many VFs at once.
NVGRE VSID Modify-Header Support	Extended packet modify-header operations to support `set` and `copy` actions on the NVGRE VSID (Virtual Subnet Identifier). A new field, `TUNNEL_HDR_DW_2` (0x84), enables dynamic VSID modification, adding header rewrite support for NVGRE tunnel traffic in addition to existing filtering capabilities.
mlxlink	mlxlink `show_links` now reports the full PCIe identifier (domain/segment + BDF), improving device-to-link mapping and avoiding ambiguous/duplicate BDF entries on multi-domain systems.

10 Legal Notices and 3rd Party Licenses

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