MFS1S00-HxxxV 200Gb/s QSFP56 MMF AOC Product Specifications

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1 Introduction

The NVIDIA® MFS1S00 is a QSFP56 VCSEL-based (Vertical Cavity Surface-Emitting Laser) active optical cable (AOC) designed for use in 200Gb/s InfiniBand (IB) HDR (High Data Rate) and 200GbE systems.

The MFS1S00 AOC offers high port density and configurability, and a much longer reach than passive copper cables in the data centers. Since the AOC is hot pluggable, it is easy to install and replace.

The MFS1S00 has a standard SFF-8665 compliant QSFP56 port on the electrical side towards the host system. It contains four multi-mode fibers (MMF) optic transceivers per end, each operating at data rates of up to 50Gb/s.

The MFS1S00 offers selectable retiming per lane for both its optical transmitters and receivers up to 50Gb/s rates.

NVIDIA's unique quality cable solutions provide power-efficient connectivity for data center interconnects. It enables higher port bandwidth, density and configurability at a low cost, and reduced power requirement in the data centers. Rigorous production testing ensures the best out-of-the-box installation experience, performance and durability.



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1.1 Key Features

- Supports IBTA IB HDR and 200GbE
- Up to 200Gb/s
- 4x 50Gb/s PAM4 modulation
- Programmable Rx output amplitude and pre-emphasis
- SFF-8665 compliant QSFP56 port
- Single 3.3V power supply
- 5.0W power consumption (typ., each end, with retiming)

- Up to 100m length
- Hot pluggable
- RoHS compliant
- SFF-8636 compliant I^2C management interface

1.2 Applications

- Supports 200Gb InfiniBand HDR Systems
- Supports 200 GbE between SN3700 and SN4600 switches

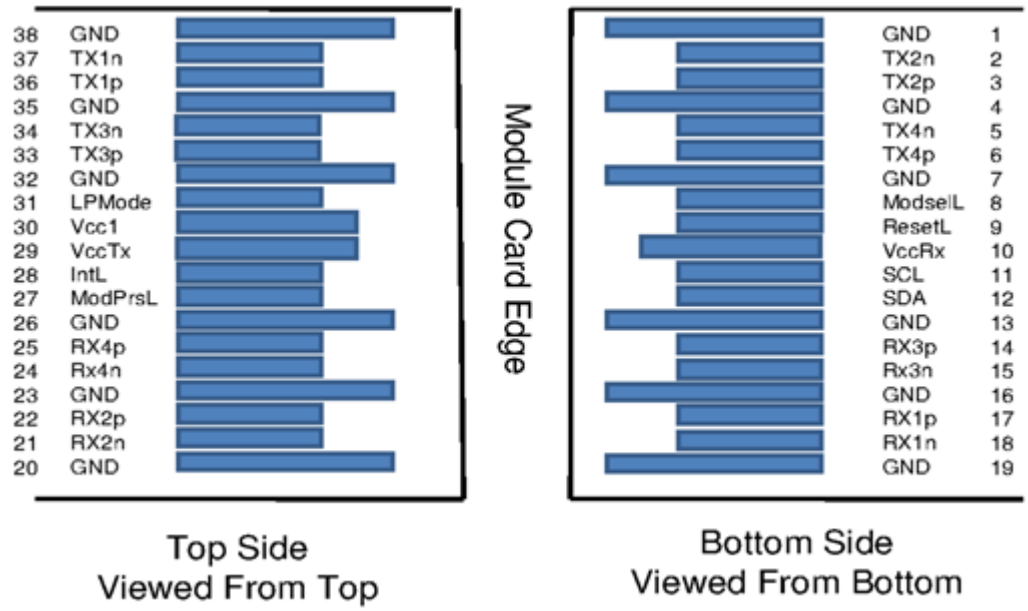
2 Pin Description

The Active Optical Cable) pin assignment is SFF-8679 compliant.

2.1 QSFP56 Pin Description

Pin	Symbol	Description	Pin	Symbol	Description
1	GND	Ground	20	GND	Ground
2	Tx2n	Transmitter Inverted Data Input	21	Rx2n	Receiver Inverted Data Output
3	Tx2p	Transmitter Non-Inverted Data Input	22	Rx2p	Receiver Non-Inverted Data Output
4	GND	Ground	23	GND	Grounds
5	Tx4n	Transmitter Inverted Data Input	24	Rx4n	Receiver Inverted Data Output
6	Tx4p	Transmitter Non-Inverted Data Input	25	Rx4p	Receiver Non-Inverted Data Output
7	GND	Ground	26	GND	Ground
8	ModSelL	Module Select	27	ModPrsL	Module Present
9	ResetL	Module Reset	28	IntL	Interrupt
10	Vcc Rx	+3.3V Power Supply Receiver	29	Vcc Tx	+3.3V Power Supply Transmitter
11	SCL	2-wire Serial Interface Clock	30	Vcc1	+3.3V Power Supply
12	SDA	2-wire Serial Interface Data	31	LPMode	Low Power Mode
13	GND	GND	32	GND	Ground
14	Rx3p	Receiver Non-Inverted Data Output	33	Tx3p	Transmitter Non-Inverted Data Input
15	Rx3n	Receiver Inverted Data Output	34	Tx3n	Transmitter Inverted Data Input
16	GND	Ground	35	GND	Ground
17	Rx1p	Receiver Non-Inverted Data Output	36	Tx1p	Transmitter Non-Inverted Data Input
18	Rx1n	Receiver Inverted Data Output	37	Tx1n	Transmitter Inverted Data Input
19	GND	Ground	38	GND	Ground

2.1.1 QSFP56 Module Pad Layout



2.2 Control Signals

This transceiver is SFF-8636 compliant. This means that the control signals shown in the pad layout support the following functions:

ModPrsL	Module Present pin, grounded inside the module. Terminated with pull-up in the host system. Asserted low when the transceiver is inserted, whereby the host detects the presence of the transceiver.
ModSelL	Module Select input pin, terminated high in the module. Only when held low by the host, the module responds to 2-wire serial communication commands. The ModSelL enables multiple modules to share a single 2-wire interface bus.
ResetL	Reset input pin, pulled high in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. During reset the host shall disregard all status bits until the module indicates completion of the reset interrupt by asserting IntL signal low with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module completes the reset interrupt without requiring a reset.
LPMode	Low Power Mode input, pulled up inside the module. The transceiver starts up in low-power mode, i.e. <1.5 W with the two-wire interface active. The host system can read the power class declaration from the transceiver and determine if it has enough power to enable the high-speed operation/high power mode of the transceiver. This can be done by asserting LPMode low or by use of the Power_over-ride and Power_set control bits (Address A0h, byte 93 bits 0,1).
IntL	Interrupt Low is an open-collector output, terminated high in the host system. A “Low” indicates a possible module operational fault or a status critical to the host system, e.g. temperature alarm. The host identifies the source of the interrupt using the 2-wire serial interface. The INTL pin is de-asserted “High” after completion of reset, when byte 2 bit 0 (Data Not Ready) is read with a value of ‘0’.

The low-speed signals are Low Voltage TTL (LVTTL) compliant (except for SCL and SDA signals).

2.3 Diagnostics and Other Features

The transceiver complies with the SFF-8665 specification and has the following key features:

Physical layer link optimization:

- Programmable Tx input equalization
- Programmable Rx output amplitude
- Programmable Rx output pre-emphasis
- Tx/Rx CDR control
  by default enabled for 100 GbE operation, disable it for 40G operation

Digital Diagnostic Monitoring (DDM):

- Rx receive optical power monitor for each lane
- Tx transmit optical power monitor for each lane
- Tx bias current monitor for each lane
- Supply voltage monitor
- Transceiver case temperature monitor
- Warning and Alarm thresholds for each DDM function (not user changeable)

Other SFF-8636 functions and interrupt indications:

- Tx & Rx LOS indication
- Tx & Rx LOL indication
- Tx fault indication

LOS, LOL, and Tx Fault status flags can be read via the two-wire management interface and are jointly transmitted via the IntL output pin. Relevant advertisement, threshold, and readout registers are found in the SFF-8636 MSA.

2.4 Handling Precautions and Electrostatic Discharge (ESD)

The MFS1S00-HxxxV is compatible with ESD levels in typical data center operating environments and certified in accordance with the standards listed in the Regulatory Compliance Section. The product is shipped with protective caps on its connectors to protect it until the time of installation. In normal handling and operation of high-speed cables and optical transceivers, ESD is of concern during insertion into the QSFP cage of the server/switch. Hence, standard ESD handling precautions must be observed. These include use of grounded wrist/shoe straps and ESD floor wherever a cable/transceiver is extracted/inserted. Electrostatic discharges to the exterior of the host equipment chassis after installation are subject to system level ESD requirements.

3 Specifications

3.1 Absolute Maximum Specifications

Absolute maximum ratings are those beyond which damage to the device may occur.

Prolonged operation between the operational specifications and absolute maximum ratings is not intended and may cause permanent device degradation.

Parameter	Min	Max	Units
Supply voltage	-0.3	3.6	V
Data input voltage	-0.3	3.465	V
Control input voltage	-0.3	4.0	V
Damage Threshold	3.4	---	dBm

3.2 Environmental Specifications

This table shows the environmental specifications for the product.

Parameter	Min	Max	Units
Storage temperature	-40	85	°C

3.3 Operational Specifications

This section shows the range of values for normal operation. The host board power supply filtering should be designed as recommended in the SFF Committee Spec.

Parameter	Min	Typ	Max	Units
Supply voltage (V_{CC})	3.135	3.3	3.465	V
Power dissipation (each end, retiming on all lanes)	---	4.8	5.0	W
Supply noise tolerance (10Hz – 10MHz)	66	---	---	mVpp
Operating case temperature	0	---	70 [1]	°C
Operating relative humidity	5	---	85	%

1. Internal temperature readout through DDMI of up to 75°C is allowed.

3.4 Electrical Specifications

Parameter	Min	Typ	Max	Units
Signaling rate	-100 ppm	53.125	+100 ppm	Gb/s (PAM4)
	-100 ppm	25.78125	+100 ppm	Gb/s (NRZ)

Parameter	Min	Typ	Max	Units
Differential data input swing at TP1a	TBD	---	900	mVpp
Differential data output swing at TP4	---	---	900	mVpp
Near-end ESMW	0.265	---	---	UI
Near-end output eye height	70	---	---	mVpp
Output transition time, 20% to 80%	9.5	---	---	ps

Notes:

- Multiple clock domains are supported only on line-side Rx. Host side Rx supports a single clock domain only.
- QSFP Tx CDR lock can only occur if Tx lane 1 is transmitting data (Does not apply to option 1).

3.5 Interoperability

For configurations tested with the AOCs, please refer to the system level product (SLP) qualification report.

3.6 Rate Select

The AOC supports rate select, which is controlled by writing to registers 0x57-0x58. Two bits are assigned for each receiver lane in byte 0x57 (87dec, Rxn_Rate_Select) and two bits for each transmitter lane in byte 0x58 (88dec, Txn_Rate_Select) to specify up to four bitrates, as defined in SFF-8636 Rev 2.9.2 Table 6-5 XN_RATE_SELECT ENCODINGS. All four lanes are required to have the same rate select value.

The below table specifies the rate for each rate select setting.

3.6.1 Rate Select Encodings

Rate Select Value	Operating Rate (GBd)
10	25.78125 NRZ (EDR)
11	26.56250 PAM4 (HDR)

3.7 Mechanical Specifications

Parameter	Value		Units
Diameter	3 +/-0.2		mm
Minimum bend radius	30		mm
Length tolerance	length < 5 m	+300 /-0	mm
	5 m ≤ length < 50 m	+500 / -0	
	50 m ≤ length	+1000 /-0	

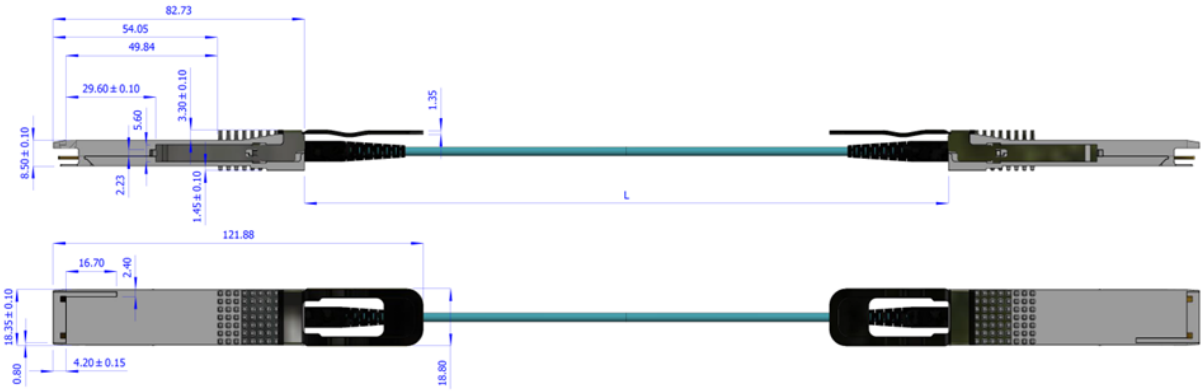
Parameter	Value	Units
Cable color	Aqua	---

3.8 Mechanical Specifications

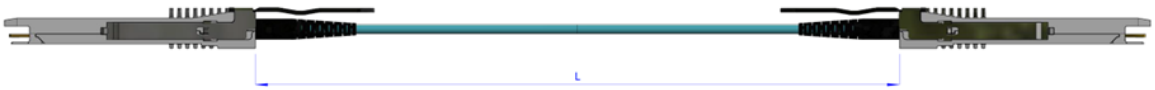
Images are for illustration purposes only. Product labels, colors, and form may vary.

Shipped packages may vary in size, artwork, raw materials and other packaging elements.

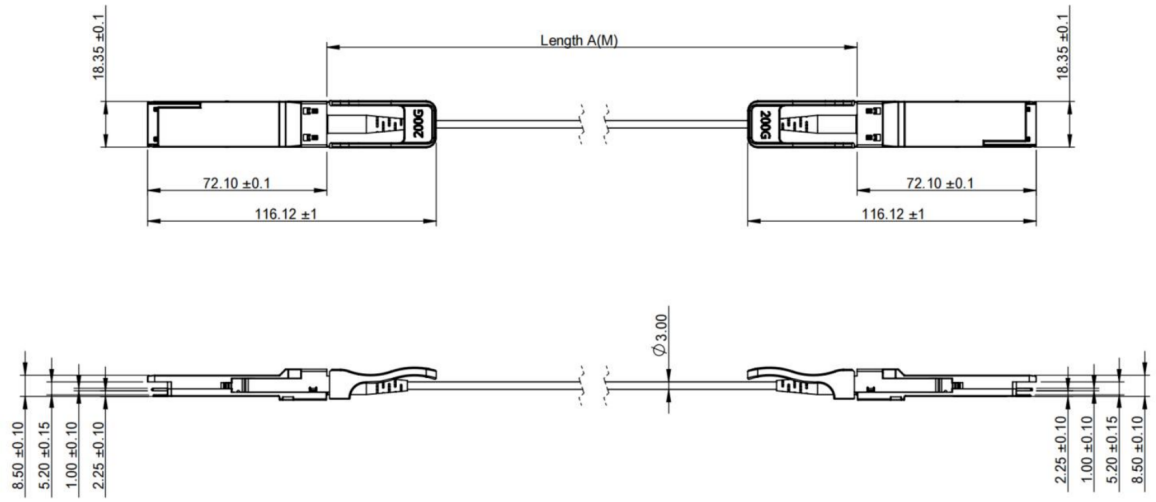
3.8.1 Mechanical Dimensions for Option 1



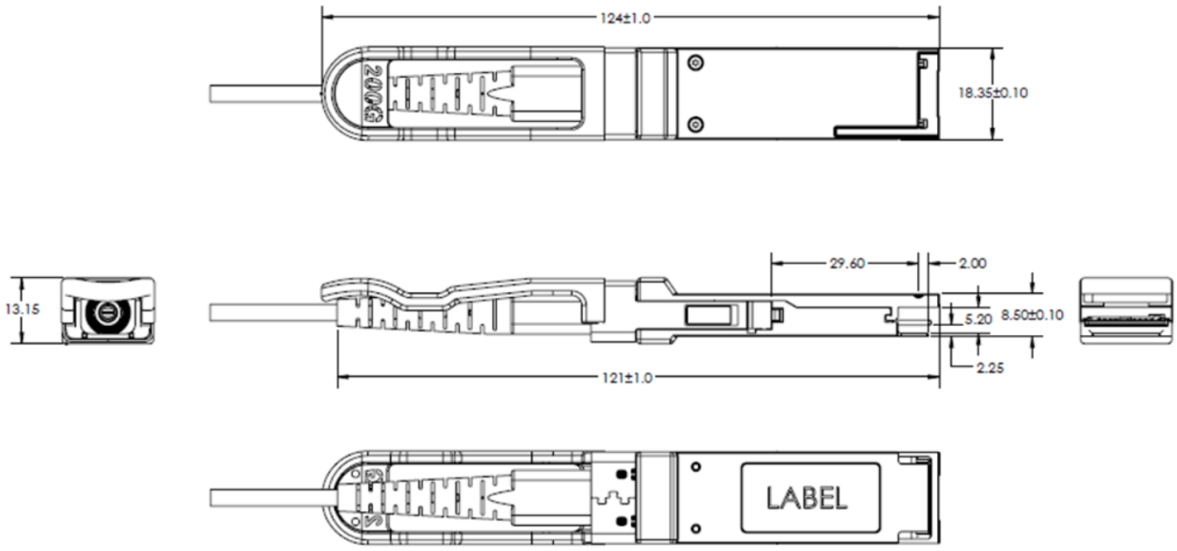
3.8.2 Cable Length Definition for Option 1



3.8.3 Mechanical Dimensions for Option 2



3.8.4 Mechanical Dimensions for Option 3

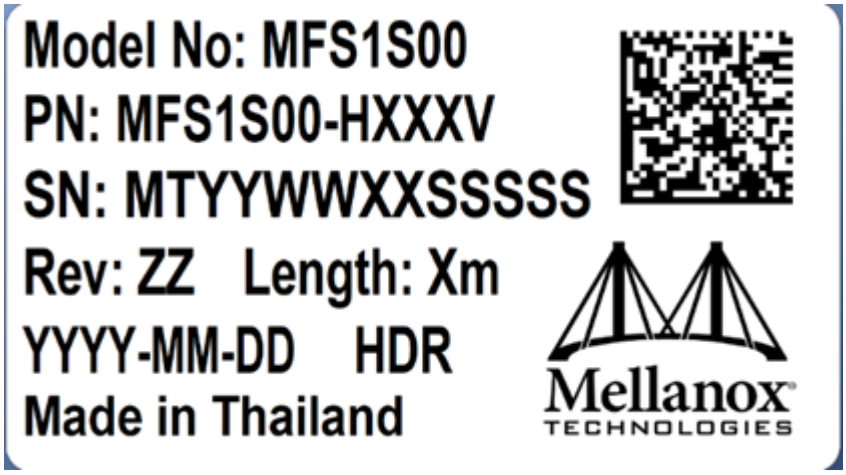


For option 3 of this product line, the earliest qualified firmware versions are E6 B1 and E6 B2.

3.8.5 Labels

The following label is applied on the transceiver's back-shell:

3.8.5.1 Backshell Label



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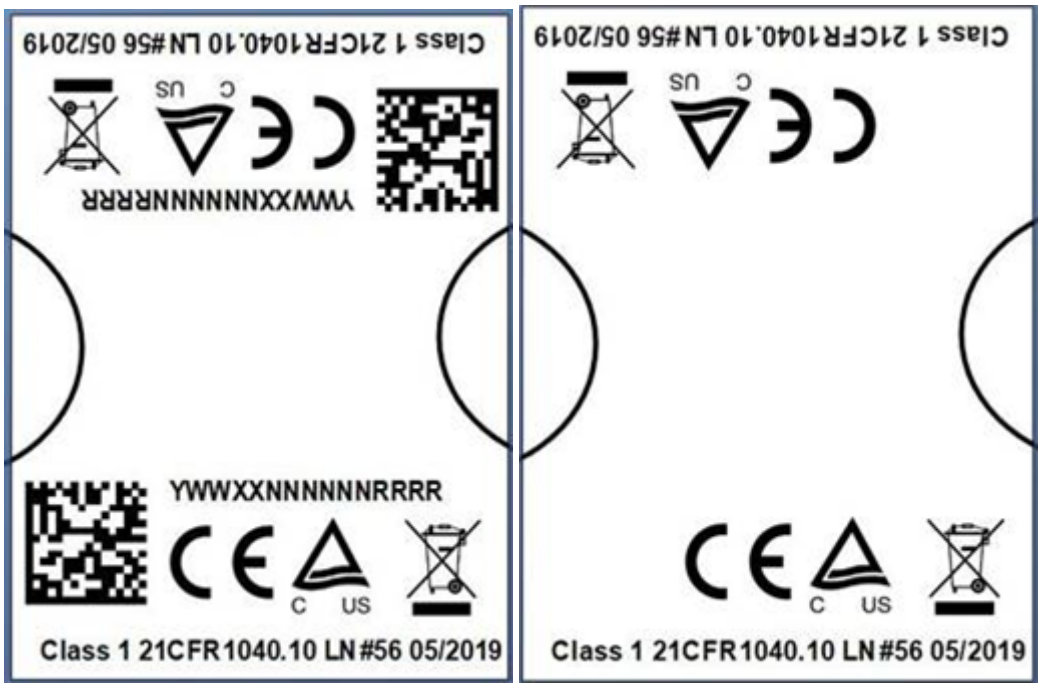
3.8.5.2 Back-Shell Label Legend

Symbol	Meaning	Notes
PN - Part Number		
xxx	Length	Meter
SN – Serial Number		
MT	Manufacturer name	2 characters, e.g. MT
YY	Year of manufacturing	2 digits
WW	Week of manufacturing	2 digits
XX	Manufacturer site	2 characters
SSSSS	Serial number	5 digits for serial number, starting from 00001. Reset at start of week to 00001.
Miscellaneous		
ZZ	HW and SW revision	2 alpha-numeric characters
Xm	Cable length	Meter
YYYY	Year of manufacturing	4 digits
MM	Month of manufacturing	2 digits
DD	Day of manufacturing	2 digits

Symbol	Meaning	Notes
COO	Country of origin	E.g. China or Thailand
	Quick response code	Serial number

The following label is applied on the cable's jacket:



The serial number and barcode are for NVIDIA internal use only. Different layouts of this label apply to different production series. It has no effect on the cable's performance nor function.
Images are for illustration purposes only. Product labels, colors, and lengths may vary.

3.8.6 Regulatory Compliance and Classification

The laser module is classified as class I according to IEC 60825-1, IEC 60825-2 and 21 CFR 1040 (CDRH).

- Safety: CB, cTUVus, CE
- EMC: CE, FCC, ICES, RCM, VCCI

Ask your NVIDIA FAE for a zip file of the certifications for this product.

3.8.7 FCC Class A Notice

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.



4 Ordering Information

Legacy OPN	NVIDIA OPN	Description
MFS1S00-H003V	980-9I457-00H003	NVIDIA active optical cable, up to 200Gbps , QSFP56 to QSFP56, 3m
MFS1S00-H005V	980-9I45D-00H005	NVIDIA active optical cable, up to 200Gbps , QSFP56 to QSFP56, 5m
MFS1S00-H010V	980-9I45J-00H010	NVIDIA active optical cable, up to 200Gbps , QSFP56 to QSFP56, 10m
MFS1S00-H015V	980-9I45O-00H015	NVIDIA active optical cable, up to 200Gbps , QSFP56 to QSFP56, 15m
MFS1S00-H020V	980-9I45T-00H020	NVIDIA active optical cable, up to 200Gbps , QSFP56 to QSFP56, 20m
MFS1S00-H030V	980-9I440-00H030	NVIDIA active optical cable, up to 200Gbps , QSFP56 to QSFP56, 30m
MFS1S00-H050V	980-9I447-00H050	NVIDIA active optical cable, up to 200Gbps , QSFP56 to QSFP56, 50m
MFS1S00-H100V	980-9I44H-00H100	NVIDIA active optical cable, up to 200Gbps , QSFP56 to QSFP56, 100m

Please see here for the cable length definition.

5 References

- QSFP Quad Small Form Factor Pluggable – Concept: SFF-8665: https://www.snia.org/technology-communities/sff/specifications
- QSFP Quad Small Form Factor Pluggable – Management: SFF-8636: https://www.snia.org/technology-communities/sff/specifications
- InfiniBand Architecture Specification and FAQ: https://www.infinibandta.org/ibta-specification/
- Environmental and Regulatory compliance statements: https://www.mellanox.com/company/quality/regulatory-compliance/environmental
- Nvidia Networking Cable Configurator: https://www.mellanox.com/products/interconnect/cables-configurator
- Nvidia Cable Management Guide and FAQ: https://mymellanox.force.com/support/servlet/fileField?id=0BE1T000000TcKC

For documentation, please contact your sales representative or the Support team.

6 Document Revision History

Revision	Date	Description
1.5	May. 2025	Updated Mechanical Dimensions for Option 3
1.4	Jan. 2024	Updated Mechanical Dimensions for Option 2
1.3	Oct. 2023	• Added 200GbE mentions • Updated ordering information table
1.2	Apr. 2022	Added a note to Mechanical Dimensions for Option 3.
1.1	Nov. 2021	Reformatted and rebranded; migrated to HTML.
1.0	Oct. 2021	First release.

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