MMA1B00-C100D 100GbE QSFP28 MMF SR4 Transceiver Product Specifications

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1 Introduction

NVIDIA® MMA1B00-C100D is a 4-channel, pluggable QSFP28 optical transceiver designed for use in 100GbE Ethernet links with up to 100 m reach on multi-mode fiber (MMF). This transceiver incorporates our integrated circuit technology to provide high performance at low power.

The MMA1B00-C100D converts 4 input channels of 25 Gb/s electrical data to 4 optical signals at 850 nm. Reversely, the receiver side de-multiplexes 4 optical inputs into 4 electrical differential output signals.
The transceiver has selectable retiming as specified in the SFF-8636 MSA. The transceiver can therefore be used in both 40 GbE and 100 GbE applications.

Digital diagnostic monitoring functions for temperature, supply voltage, and optical power are available via the two-wire (I2C) management interface, as specified by the QSFP28 MSA.

The optical interface is a Multi-fiber Push-On (MPO) connector with four optical channels/fibers in each direction. The MPO connector is un-angled (UPC).

Rigorous production testing ensures the best out-of-the-box installation experience, performance, and durability.

Rev. A4 or lower	Rev. B1 or Higher
	

⚠ Images are for illustration purposes only. Product labels, colors, and lengths may vary.

1.1 Key Features

- Up to 100Gb/s
- Selectable retiming for both Tx and Rx
- Programmable Tx input equalizer
- Programmable Rx output amplitude and emphasis
- SFF-8665 compliant QSFP28
- Single 3.3V supply, hot pluggable
- QSFP28 power class 3 (2.5 W max)
- 2.2 W power consumption (typ, with retiming)
- Class 1 laser safety
- Up to 100m on OM4, and 70m on OM3 multimode fiber at 100 Gb/s
- Up to 100m on OM3 at 40 Gb/s

- SFF-8636 compliant DDM
- Hot pluggable
- RoHS compliant

1.2 Applications

- 100GBASE-SR4 100G Ethernet
- 40GBASE-SR4 40G Ethernet
- Qualified for use in NVIDIA Ethernet end-to-end systems

2 Pin Description

2.1 QSFP28 Pin Function Description

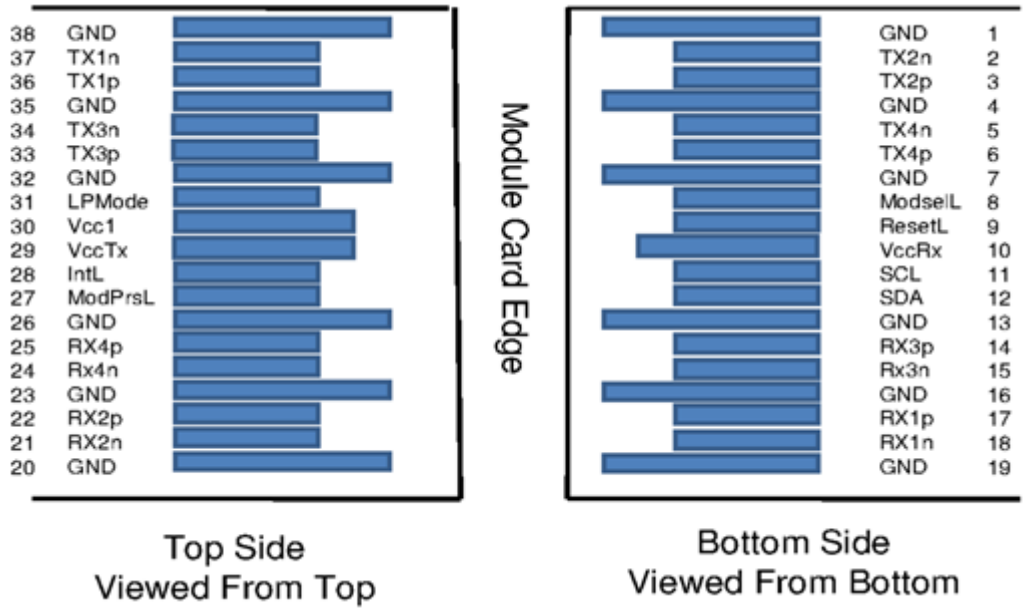
The transceiver's pin assignment is SFF-8679 compliant.

Pin	Symbol	Description	Pin	Symbol	Description
1	GND	Ground	20	GND	Ground
2	Tx2n	Transmitter Inverted Data Input	21	Rx2n	Receiver Inverted Data Output
3	Tx2p	Transmitter Non-Inverted Data Input	22	Rx2p	Receiver Non-Inverted Data Output
4	GND	Ground	23	GND	Grounds
5	Tx4n	Transmitter Inverted Data Input	24	Rx4n	Receiver Inverted Data Output
6	Tx4p	Transmitter Non-Inverted Data Input	25	Rx4p	Receiver Non-Inverted Data Output
7	GND	Ground	26	GND	Ground
8	ModSelL	Module Select	27	ModPrsL	Module Present
9	ResetL	Module Reset	28	IntL	Interrupt
10	Vcc Rx	+3.3V Power Supply Receiver	29	Vcc Tx	+3.3V Power Supply Transmitter
11	SCL	2-wire Serial Interface Clock	30	Vcc1	+3.3V Power Supply
12	SDA	2-wire Serial Interface Data	31	LPMode	Low Power Mode
13	GND	GND	32	GND	Ground
14	Rx3p	Receiver Non-Inverted Data Output	33	Tx3p	Transmitter Non-Inverted Data Input
15	Rx3n	Receiver Inverted Data Output	34	Tx3n	Transmitter Inverted Data Input
16	GND	Ground	35	GND	Ground
17	Rx1p	Receiver Non-Inverted Data Output	36	Tx1p	Transmitter Non-Inverted Data Input
18	Rx1n	Receiver Inverted Data Output	37	Tx1n	Transmitter Inverted Data Input
19	GND	Ground	38	GND	Ground

Notes:

- GND is the symbol for signal and supply (power) common for the QSFP28 module. All are common within the module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.
- VccRx, Vcc1 and VccTx are the receiving and transmission power suppliers and shall be applied concurrently.
- Vcc Rx, Vcc1 and Vcc Tx may be internally connected within the module in any combination. The connector pins are each rated for a maximum current of 1000 mA.

2.1.1 QSFP28 Module Pad Layout



2.2 Control Signals

This transceiver is SFF-8636 compliant. This means that the control signals shown in the pad layout support the following functions:

Name	Function	Description
ModPrsL	Output, asserted low	Module Present pin, grounded inside the module. Terminated with pull-up in the host system. Asserted low when the transceiver is inserted, whereby the host detects the presence of the transceiver.
ModSelL	Input, asserted Low	Module Select input pin, terminated high in the module. Only when held low by the host, the module responds to 2-wire serial communication commands. The ModSelL enables multiple modules to share a single 2-wire interface bus.

Name	Function	Description
ResetL	Input, asserted Low	Reset input pin, pulled high in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. During reset the host shall disregard all status bits until the module indicates completion of the reset interrupt by asserting IntL signal low with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module completes the reset interrupt without requiring a reset.
LPMode	Input, asserted high	Low Power Mode input, pulled up inside the module. The transceiver starts up in low-power mode, i.e. <1.5 W with the two-wire interface active. The host system can read the power class declaration from the transceiver and determine if it has enough power to enable the high-speed operation/high power mode of the transceiver. This can be done by asserting LPMode low or by use of the Power_over-ride and Power_set control bits (Address A0h, byte 93 bits 0,1).
IntL	Output, asserted low	Interrupt Low is an open-collector output, terminated high in the host system. A “Low” indicates a possible module operational fault or a status critical to the host system, e.g. temperature alarm. The host identifies the source of the interrupt using the 2-wire serial interface. The INTL pin is de-asserted “High” after completion of reset, when byte 2 bit 0 (Data Not Ready) is read with a value of ‘0’.

The low-speed signals are Low Voltage TTL (LVTTL) compliant (except for SCL and SDA signals).

2.3 Diagnostics and Other Features

The transceiver complies with the SFF-8665 specification and has the following key features:

Physical layer link optimization:

- Programmable Tx input equalization
- Programmable Rx output amplitude
- Programmable Rx output pre-emphasis
- Tx/Rx CDR control
  by default enabled for 100 GbE operation, disable it for 40G operation

Digital Diagnostic Monitoring (DDM):

- Rx receive optical power monitor for each lane
- Tx transmit optical power monitor for each lane
- Tx bias current monitor for each lane
- Supply voltage monitor
- Transceiver case temperature monitor
- Warning and Alarm thresholds for each DDM function (not user changeable)

Other SFF-8636 functions and interrupt indications:

- Tx & Rx LOS indication

- Tx & Rx LOL indication
- Tx fault indication

LOS, LOL, and Tx Fault status flags can be read via the two-wire management interface and are jointly transmitted via the IntL output pin. Relevant advertisement, threshold, and readout registers are found in the SFF-8636 MSA.

3 Specifications

3.1 Absolute Maximum Specifications

Absolute maximum ratings are those beyond which permanent damage to the device may occur.

Parameter	Min	Max	Units
Supply voltage	-0.3	3.6	V
Data input voltage	-0.3	3.465	V
Control input voltage	-0.3	4	V
Damage Threshold, per optical lane	3.4	---	dBm
Storage temperature	-40	85	°C

3.2 Recommended Operating Conditions and Power Supply Requirements

Parameter	Min	Typ	Max	Units
Supply voltage	3.135	3.3	3.465	V
Power consumption (no retiming)	---	1.5	1.8	W
Power consumption (retiming on all lanes)	---	2.2	2.5	W
Supply noise tolerance (10 Hz – 10 MHz)	66	---	---	mVpp
Operating case temperature	0	---	70	°C
Operating relative humidity	5	---	85	%

3.3 Electrical Specifications

Parameter (per lane)	Min	Typ	Max	Units	Notes
Signaling rate (with retiming)	-100ppm	25.78125	+100ppm	Gb/s	---
Signaling rate (without retiming)	0.3		25.784	Gb/s	---
Transmitter					
Differential data input swing at TP1a	IEEE 802.3bm 83E.3.4.1	---	900	mVpp	1
Differential input return loss	Meets equation (83E–5) in IEEE 802.3bm			dB	---
Receiver					
Differential output return loss	Meets equation (83E–5) in IEEE 802.3bm			dB	---
Differential data output swing at TP4	300	---	480	mVpp	---
Common mode output return loss	---	---	-6	dB	---

Parameter (per lane)	Min	Typ	Max	Units	Notes
Output eye width (EW15)	0.57	---	---	UI	---
Output eye height (EH15)	228	---	---	mV	---
Output transition time, 20 to 80%	17	---	---	ps	---
Output eye crossing	45	---	---	%	---

Note 1: Min requires optimization of the input equalizer.

3.4 Optical Specifications

Parameter	Min	Typ	Max	Units	Notes
Transmitter (per lane)					
Signaling speed (with retiming)	-100ppm	25.78125	+100ppm	Gb/s	---
Signaling speed (without retiming)	0.3	---	25.7840	Gb/s	---
Center wavelength	840	---	860	nm	---
Average launch power	-8.4	---	2.4	dBm	---
Transmit OMA	-6.4	---	3	dBm	---
Extinction Ratio	2	---	---	dB	---
Transmitter and dispersion eye closure	---	---	4.3	dB	---
Average launch power at Tx squelched	---	---	-30	dBm	---
Eye crossing	45	---	55	%	---
Optical return loss tolerance	---	---	12	dB	---
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3} Hit ratio $1.5 \cdot 10^{-3}$ hits per sample	{0.3, 0.38, 0.45, 0.35, 0.41, 0.5}			---	
Reach on OM3 multi-mode fiber	70	---	---	m	---
Reach on OM4 multi-mode fiber	100	---	---	m	---
Receiver (per lane)					
Signaling speed (with retiming)	-100ppm	25.78125	+100ppm	Gb/s	---
Signaling speed (without retiming)	0.3	---	25.784	Gb/s	---
Center wavelength	840	---	860	nm	---
Receiver reflectance	---	---	-12	dB	---
LOS de-Assert	---	---	-12	dBm	---
LOS assert	-30	---	---	dBm	---
LOS hysteresis	0.5	---	---	dB	---
Unstressed receiver sensitivity (OMA) at BER 10^{-12}	---	---	-7	dBm	1, 4
Stressed receiver sensitivity (OMA), each lane	---	---	-5.2	dBm	2

Parameter	Min	Typ	Max	Units	Notes
Conditions for stressed receiver sensitivity	See below				3
Test Conditions					
Stressed eye closure (SEC), lane under test	4.3			dB	---
Stressed eye J2 Jitter, lane under test	0.39			UI	---
Stressed eye J4 Jitter, lane under test (max)	0.53			UI	---
OMA of each aggressor lane	3			dBm	---
Stressed receiver eye mask definition {X1, X2, X3, Y1, Y2, Y3} Hit ratio 5 x 10^{-5} hits per sample	{0.28, 0.5, 0.5, 0.33, 0.33, 0.4}			---	---

Notes:

1. All Tx channels on and all Rx channels on with AOP 3dB greater than the tested channel. Injected optical eye must comply with the transmitter eye mask definition from the table.
2. Measured with conformance test signal at TP3 (ref. IEEE 802.3 100GBASE-SR4) for BER < $5{\cdot}10^{-5}$
3. The test conditions are for measuring stressed receiver sensitivity only – not characteristics of the receiver.
4. For revision A4 or lower, Max is -6dBm.

3.5 Electrostatic Discharge (ESD)

This product is compatible with ESD levels in typical data center operating environments and certified in accordance with the standards listed in the Regulatory Compliance Section. The product is shipped with protective caps on all connectors to protect it during shipping. In normal handling and operation of high-speed cables and optical transceivers, ESD is of concern during insertion into the OSFP cage of the server/switch. Hence, standard ESD handling precautions must be observed. These include use of grounded wrist/shoe straps and ESD floor wherever a cable/transceiver is extracted/inserted. Electrostatic discharges to the exterior of the host equipment chassis after installation are subject to system level ESD requirements.

3.6 Handling and Cleaning

The transceiver can be damaged by exposure to current surges and over voltage events. Take care to restrict exposure to the conditions defined in Absolute Maximum Ratings. Observe normal handling precautions for electrostatic discharge-sensitive devices. The transceiver is shipped with dust caps on both the electrical and the optical port. The cap on the optical port should always be in place when there is no fiber cable connected. The optical connector has a recessed connector surface which is exposed whenever it has no cable nor cap.

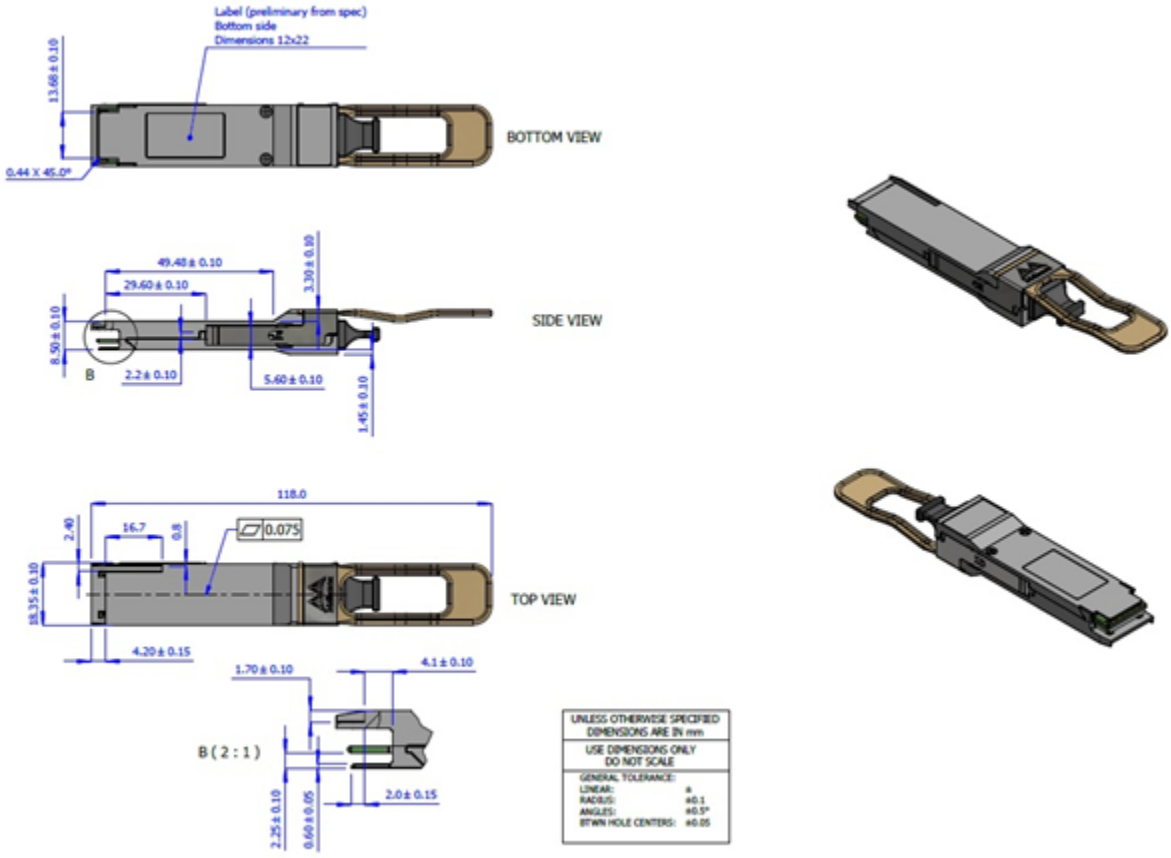
Prior to insertion of the fiber cable, clean the cable connector to prevent contamination from it. The dust cap ensures that the optics remain clean and no additional cleaning should be needed. In the event of contamination, standard cleaning tools and methods should be used. Liquids must not be applied.

3.7 Mechanical Specifications

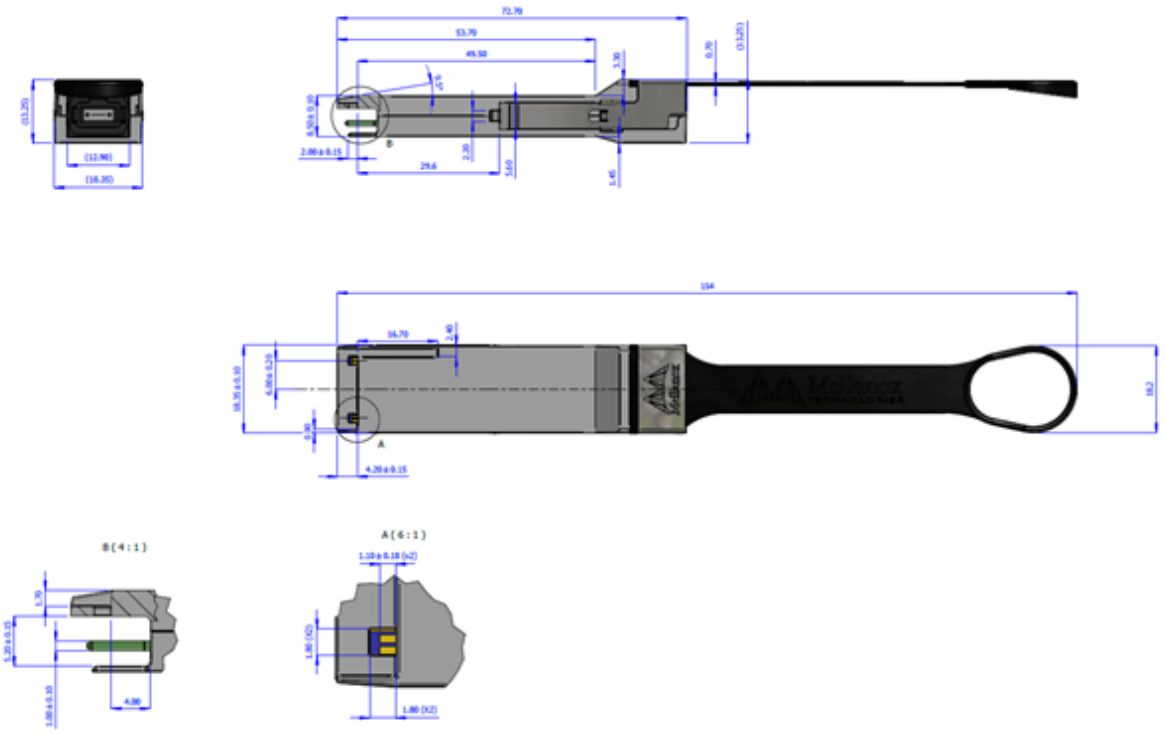
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⚠ Shipped packages may vary in size, artwork, raw materials and other packaging elements.

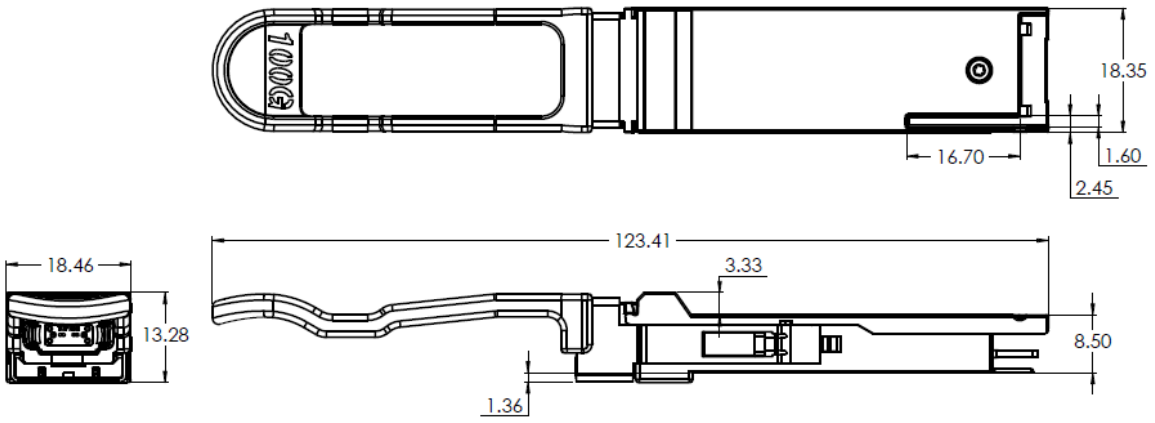
Mechanical Dimensions Rev. B1 and Higher



Mechanical Dimensions Rev. A4 and Lower



Alternate source mechanical dimentions

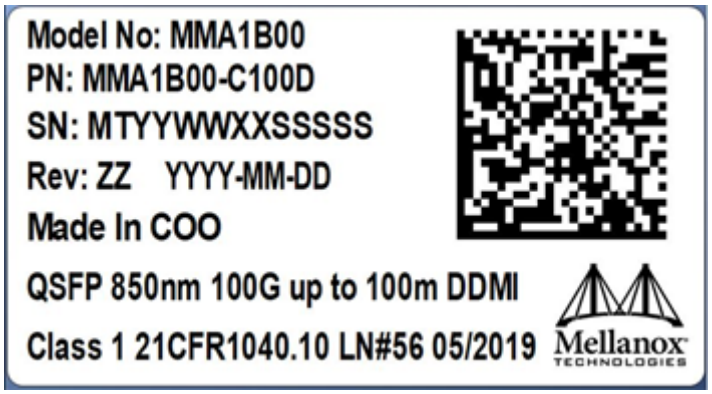


3.7.1 Memory Map

The transceiver's memory map is compliant with the QSFP Management interface specification SFF-8636. See also NVIDIA LinkX® Memory Map Application Note (MLNX-15-5926).

3.7.2 Label

The following label is applied on the transceiver's backshell:



(sample illustration)

3.7.2.1 Backshell Label Legend

Symbol	Meaning	Notes
SN – Serial Number		
MT	Manufacturer name	2 characters (MT)
YY	Year of manufacturing	2 digits
WW	Week of manufacturing	2 digits
DM	Manufacturer site	2 characters
ZZZZZ	Serial number	5 digits for serial number, starting from 00001. Reset at start of week to 00001.
Miscellaneous		
ZZ	HW and SW revision	2 alpha-numeric characters
YYYY	Year of manufacturing	4 digits
MM	Month of manufacturing	2 digits
DD	Day of manufacturing	2 digits
COO	Country of origin	E.g. China or Malaysia
	Quick response code	Serial number (MTYYWWXXSSSSS)

3.7.3 Regulatory Compliance and Classification

The laser module is classified as class I according to IEC 60825-1, IEC 60825-2 and 21 CFR 1040 (CDRH).

- Safety: FDA/CDRH, TUV, UL/CSA, ACMA
- EMC: ITL

Ask your NVIDIA FAE for a zip file of all the certifications for this product.

3.7.4 FCC Class A Notice

Each of the devices complies with CFR47 FCC Class A Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference.
2. This device must accept any interference received, including interference that may cause undesired operation.

Note: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur during installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/television technician for help.

Modifications: Any modifications made to this device that are not approved by NVIDIA may void the authority granted to the user by the FCC to operate this equipment.



4 Ordering Information

Legacy OPN	NVIDIA OPN	Description
MMA1B00-C100D	980-9I149-00CS00	Transceiver, 100GbE, QSFP28, MPO, 850nm, SR4, up to 100m, DDMI

5 Document Revision History

Version	Date	Description of Change
1.8	Jul. 2025	Added alternate source mechanical drawings.
1.7	Nov. 2021	Reformatted and rebranded; migrated to HTML.
1.6	Apr. 2021	Removed “BER better than 10^{-15}” from Key Features. Added Electrostatic Discharge (ESD) and Handling and Cleaning sections. Updated Transmit OMA, Extinction Ratio, and Transmitter and dispersion eye closure values in the Optical Specifications table. Updated document template, legal notice, and introduction.
1.5	Nov. 2020	Added: Control Signals description, optical connector interface information in Appendix A and added References section. Updated DDM info under Diagnostics and Other Features and the Regulatory Compliance and Classification list. Minor text edits. Updated Label.
1.4	Sep. 25, 2017	Updated the Absolute Maximum Ratings table – Supply voltage Max changed from 3.465 to 3.6V.
1.1 - 1.3	Aug. 2016-2017	Refer to rev. 1.5 of this datasheet for the changes.
1.0	March 2016	Initial release

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