MMS1V00-WM 400GbE QSFP-DD DR4 Transceiver Product Specifications

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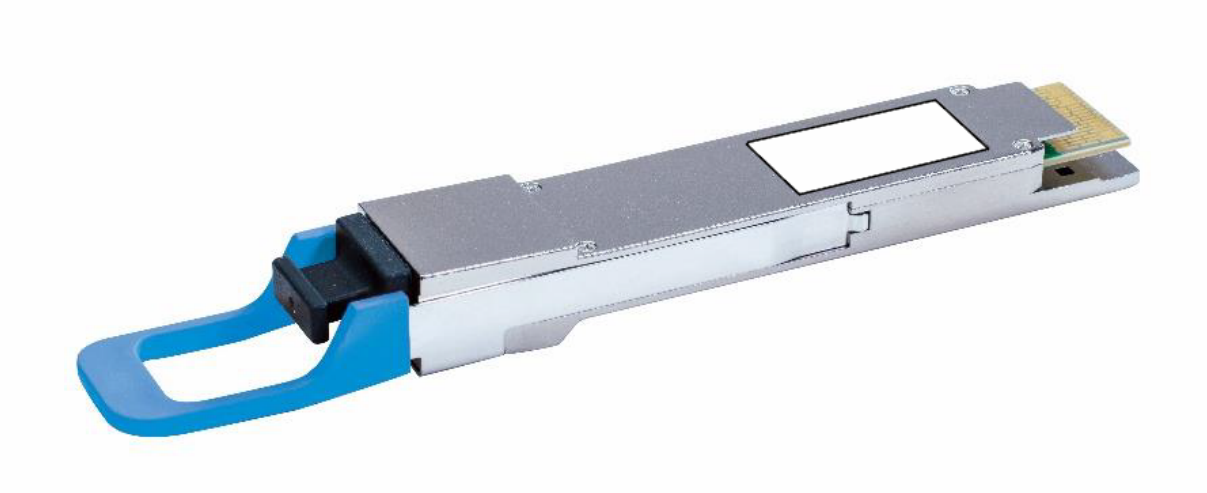
1 Introduction

The NVIDIA MMS1V00-WM transceiver is a single-mode 4-channel (DR4) QSFP-DD optical transceiver, designed for 400 Gigabit Ethernet (GbE) links on up to 500m of single mode fiber.

The MMS1V00-WM converts 8 input channels of 50Gb/s PAM4 electrical data to 4 channels of 100Gb/s PAM4 optical signals, using a nominal wavelength of 1310nm, for 400Gb/s optical transmission.

The transceiver has a standard QSFP-DD connector on the electrical side towards the host system. The optical interface is composed of four optical channels/fibers in each direction, intended for a parallel single-mode optical cable via a standard MPO connector.

Rigorous production testing ensures the best out-of-the-box installation experience, performance, and durability.



⚠ Images are for illustration purposes only. Product labels and colors may vary.

1.1 Key Features

- 2x wire serial interface with digital diagnostic monitoring
- Operating case temperature 0-70°C
- Maximum power consumption 12W
- 500m reach
- MPO12/APC optical connector
- Compliant with IEEE 802.3bs-2017 standard:
  - 400GBASE-DR4 optical interface
  - 400GAUI-8 electrical interface
- QSFP-DD MSA HW Rev 5.0; Type 2 housing with MPO-12 connector compliant
- QSFP-DD CMIS Rev 4.0 compliant
- Complies with EU Directive 2011/65/EU (RoHS compliant)

1.2 Applications

- 400GbE Ethernet systems
- Campus networks – up to 500 m reach
- Supports 4x MMS1V70-CM on MSN2700 to a single MMS1V00-WM on MSN4700 and MMS1V00-WM on MSN4700 to MMS1V00-WM on MSN4700

2 Pin Description

2.1 QSFP-DD Pin Description

The transceiver's pin assignment is SFF-8679 compliant.

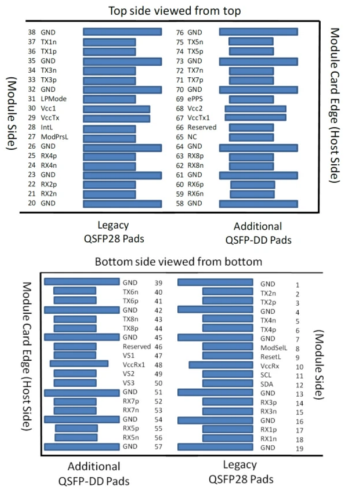
Pin	Symbol	Description	Pin	Symbol	Description
1	GND	Ground	39	GND	Ground
2	Tx2n	Transmitter Inverted Data Input	40	Tx6n	Transmitter Inverted Data Input
3	Tx2p	Transmitter Non-Inverted Data Input	41	Tx6p	Transmitter Non-Inverted Data Input
4	GND	Ground	42	GND	Ground
5	Tx4n	Transmitter Inverted Data Input	43	Tx8n	Transmitter Inverted Data Input
6	Tx4p	Transmitter Non-Inverted Data Input	44	Tx8p	Transmitter Non-Inverted Data Input
7	GND	Ground	45	GND	Ground
8	ModSelL	Module Select	46	Reserved	For future use
9	ResetL	Module Reset	47	VS1	Module Vendor Specific 1
10	Vcc Rx	+3.3V Power Supply Receiver	48	VccRx1	3.3V Power Supply
11	SCL	2-wire Serial Interface Clock	49	VS2	Module Vendor Specific 2
12	SDA	2-wire Serial Interface Data	50	VS3	Module Vendor Specific 3
13	GND	GND	51	GND	Ground
14	Rx3p	Receiver Non-Inverted Data Output	52	Rx7p	Receiver Non-Inverted Data Output
15	Rx3n	Receiver Inverted Data Output	53	Rx7n	Receiver Inverted Data Output
16	GND	Ground	54	GND	Ground
17	Rx1p	Receiver Non-Inverted Data Output	55	Rx5p	Receiver Non-Inverted Data Output
18	Rx1n	Receiver Inverted Data Output	56	Rx5n	Receiver Inverted Data Output
19	GND	Ground	57	GND	Ground
20	GND	Ground	58	GND	Ground
21	Rx2n	Receiver Inverted Data Output	59	Rx6n	Receiver Inverted Data Output
22	Rx2p	Receiver Non-Inverted Data Output	60	Rx6p	Receiver Non-Inverted Data Output
23	GND	Grounds	61	GND	Ground
24	Rx4n	Receiver Inverted Data Output	62	Rx8n	Receiver Inverted Data Output

Pin	Symbol	Description	Pin	Symbol	Description
25	Rx4p	Receiver Non-Inverted Data Output	63	Rx8p	Receiver Non-Inverted Data Output
26	GND	Ground	64	GND	Ground
27	ModPrsL	Module Present	65	NC	No Connect
28	IntL	Interrupt	66	Reserved	For future use
29	Vcc Tx	+3.3V Power Supply Transmitter	67	VccTx1	3.3V Power Supply
30	Vcc1	+3.3V Power Supply	68	Vcc2	3.3V Power Supply
31	LPMode	Low Power Mode	69	Reserved	For Future Use
32	GND	Ground	70	GND	Ground
33	Tx3p	Transmitter Non-Inverted Data Input	71	Tx7p	Transmitter Non-Inverted Data Input
34	Tx3n	Transmitter Inverted Data Input	72	Tx7n	Transmitter Inverted Data Input
35	GND	Ground	73	GND	Ground
36	Tx1p	Transmitter Non-Inverted Data Input	74	Tx5p	Transmitter Non-Inverted Data Input
37	Tx1n	Transmitter Inverted Data Input	75	Tx5n	Transmitter Inverted Data Input
38	GND	Ground	76	GND	Ground

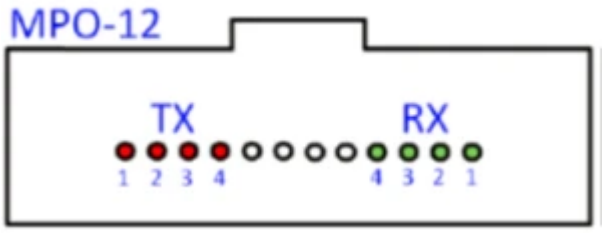
Notes:

1. GND is the symbol for signal and supply (power) common for the QSFP modules. All are common within the module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.
2. VccRx, Vcc1 and VccTx are the receiving and transmission power suppliers and shall be applied concurrently. Recommended host board power supply filtering see SFF-8679.

2.1.1 Pin *definitions* of the module high speed inputs/ outputs



2.1.2 Active fiber ports in MPO12 *connector* on module side



Note: For best performance and least amount of reflections use the angle-polished connector (APC) type.

2.2 Control Signals

This transceiver is CMIS 4.0 compliant. The control signals shown in the pad layout are implemented with the following functions:

Name	Function	Description
ModPrsL	Output, asserted low	Pull-up by host when no transceiver/cable is present. Connected to ground inside the transceiver. Hence, asserted low when a transceiver/cable is plugged in.
ModSelL	Input, asserted Low	Module Select input pin, terminated high in the module. Only when held low by the host, the module responds to 2-wire serial communication commands. The ModSelL enables multiple modules to share a single 2-wire interface bus.
ResetL	Input, asserted Low	Reset input pin, pulled high in the module. A low level on the ResetL pin for longer than the minimum length initiates a module reset. When de-asserted the transceiver starts its initialization procedure. See the CMIS specification [1] for details.
LPMode	Input, asserted high	Low Power Mode input, pulled up inside the module. Hardware control signal for forcing the transceiver into low-power state. Can be overwritten by low-power mode command.
ePPS	Input	not implemented
IntL	Output, asserted low	Interrupt Low is an open-collector output, terminated high in the host system. A “Low” indicates a possible module operational fault or a status critical to the host system, e.g. temperature alarm. The host identifies the source of the interrupt using the 2-wire serial interface.

2.3 Diagnostics and Other Features

The transceiver complies with the SFF-8665 specification and has the following key features:

Physical layer link optimization:

- Programmable Tx input equalization
- Programmable Rx output amplitude
- Programmable Rx output pre-emphasis
- Tx/Rx CDR control
  by default enabled for 200 Gb/s operation.

Digital Diagnostic Monitoring (DDM):

- Rx receive optical power monitor for each lane
- Tx transmit optical power monitor for each lane
- Tx bias current monitor for each lane
- Supply voltage monitor
- Transceiver case temperature monitor
- Warning and Alarm thresholds for each DDM function (not user changeable)

Other SFF-8636 functions and interrupt indications:

- Tx & Rx LOS indication
- Tx & Rx LOL indication
- Tx fault indication

LOS, LOL, and Tx Fault status flags can be read via the two-wire management interface and are jointly transmitted via the IntL output pin. Relevant advertisement, threshold, and readout registers are found in the CMIS 4.0 MSA.

2.4 Handling and Cleaning

The transceiver can be damaged by exposure to current surges and over voltage events. Take care to restrict exposure to the conditions defined in Absolute Maximum Ratings. Observe normal handling precautions for electrostatic discharge-sensitive devices. The transceiver is shipped with dust caps on both the electrical and the optical port. The cap on the optical port should always be in place when there is no fiber cable connected. The optical connector has a recessed connector surface which is exposed whenever it has no cable nor cap. Prior to insertion of the fiber cable, clean the cable connector to prevent contamination from it. The dust cap ensures that the optics remain clean, and no additional cleaning should be needed. In the event of contamination, standard cleaning tools and methods should be used. Liquids must not be applied.

3 Specifications

3.1 Absolute Maximum Specifications

Absolute maximum ratings are those beyond which damage to the device may occur.

Prolonged operation between the operational specifications and absolute maximum ratings is not intended and may cause permanent device degradation.

Parameter	Symbol	Min	Max	Units
Storage Temperature	T_S	-40	85	°C
Operating Case Temperature	T_{OP}	0	70	°C
Supply Voltage	Vcc	-0.5	3.6	V
Relative Humidity (non-condensing)	RH – Option 1	5	95	%
Control Input Voltage	V_I	-0.3	Vcc+0.5	V

3.2 Operational Specifications

This section shows the range of values for normal operation.

Parameter	Symbol	Min	Typ	Max	Units
Power Supply Voltage	VCC	3.135	3.3	3.465	V
Instantaneous peak current at hot plug	ICC_IP	-	-	4800	mA
Sustained peak current at hot plug	ICC_SP	-	-	3960	mA
Maximum Power Dissipation	PD	-	-	12	W
Maximum Power Dissipation, Low Power Mode	PDLP	-	-	1.5	W
Signaling Rate per Lane	SRL	-	53.125	-	GBd
Two Wire Serial Interface Clock Rate	-	-	-	400	kHz
Power Supply Noise Tolerance (10Hz - 10MHz)	-	-	-	66	mV
Rx Differential Data Output Load	-	-	100	-	Ohm
Operating Distance	-	2	-	500	m

3.3 Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Units
Transmitter (each Lane)					
Differential pk-pk input Voltage tolerance		900	-	-	mV
Differential termination mismatch		-	-	10	%
Single-ended voltage tolerance range		-0.4	-	3.3	V

Parameter	Symbol	Min	Typical	Max	Units
DC common mode Voltage		-350	-	2850	mV
Receiver (each Lane)					
AC common-mode output Voltage (RMS)		-	-	17.5	mV
Differential output Voltage		-	-	900	mV
Near-end Eye height, differential		70	-	-	mV
Far-end Eye height, differential		30	-	-	mV
Far end pre-cursor ratio		-4.5	-	2.5	%
Differential Termination Mismatch		-	-	10	%
Transition Time (min, 20% to 80%)		9.5	-	-	ps
DC common mode Voltage		-350	-	2850	mV

3.3.1 Notes:

1. Amplitude customization beyond these specs is dependent on validation in customer system.

3.3.2 Electrical Specification Low Speed Signal (compliant with QSFP-DD HW Rev 5.0)

Parameter	Symbol	Min	Max	Units
Module output SCL and SDA	VOL	0	0.4	V
	VOH	VCC-0.5	VCC+0.3	V
Module Input SCL and SDA	VIL	-0.3	VCC*0.3	V
	VIH	VCC*0.7	VCC+0.5	V
InitMode, ResetL and ModSelL	VIL	-0.3	0.8	V
	VIH	2	VCC+0.3	V
IntL	VOL	0	0.4	V
	VOH	VCC-0.5	VCC+0.3	V

3.4 Optical Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Transmitter						
Wavelength	λC	1304.5	1311	1317.5	nm	
Side Mode Suppression Ratio	SMSR	30	-	-	dB	
Average Launch Power, each lane	AOPL	-2.9	-	4.0	dBm	1

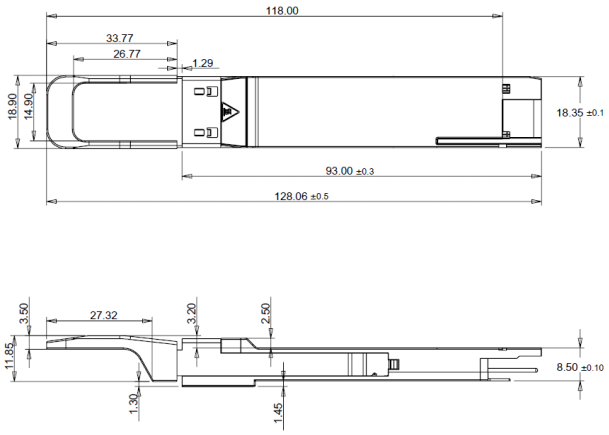
Parameter	Symbol	Min	Typ	Max	Unit	Notes
Outer Optical Modulation Amplitude (OMAouter), each lane	TOMA	-0.8	-	4.2	dBm	2
Launch Power in OMAouter minus TDECQ, each lane	TOMA-TDECQ	-2.2	-	-	dBm	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each lane	TDECQ	-	-	3.4	dB	
Average Launch Power of OFF Transmitter, each lane	TOFF	-	-	-15	dBm	
Extinction Ratio, each lane	ER	3.5	-	-	dB	
RIN21.4OMA	RIN	-	-	-136	dB/Hz	
Optical Return Loss Tolerance	ORL	-	-	21.4	dB	
Transmitter Reflectance	TR	-	-	-26	dB	3
Receiver						
Signaling rate (each lane (range)		26.5625± 100 ppm			GBd	
Modulation format		PAM4				
Wavelength	λC	1304.5	1311	1317.5	nm	
Damage Threshold, each lane	AOPD	5	-	-	dBm	
Average Receive Power, each lane	AOPR	-5.9	-	4.0	dBm	
Receive Power (OMAouter), each lane	OMAR	-	-	4.2	dBm	
Receiver Reflectance	RR	-	-	-26	dB	
Receiver Sensitivity (OMAouter), each lane	SOMA	-	-	-4.4	dBm	4
Stressed Receiver Sensitivity (OMAouter), each lane	SRS	-	-	-1.9	dBm	5
Conditions of stressed receiver sensitivity test						
Stressed eye closure for PAM4 (SECQ)			3.4		dB	
OMAouter of each aggressor lane			4.2		dBm	

Notes:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength.
2. Even if TDECQ < 1.4dB, OMAouter (min) must exceed this value.
3. Transmitter reflectance is defined looking into the transmitter.
4. Receiver sensitivity (OMAouter), each lane (max) is informative and is defined for a transmitter with SECQ of 0.9 dB.
5. Measured with conformance test signal at TP3 for the BER = $2.4x10^{-4}$.

3.5 Mechanical Specifications

3.5.1 Mechanical Dimensions



3.6 Label

The label applied on the transceiver's backshell is illustrated below.

3.6.1 Backshell Label



Images are for illustration purposes only. Product labels, colors, and form may vary.

3.6.2 Transceiver Backshell Label Serial Number Legend

Symbol	Meaning	Notes
SN – Serial Number		
MT	Manufacturer name	2 characters, e.g. MT
YY	Year of manufacturing	2 digits
WW	Week of manufacturing	2 digits
JC	Manufacturer site	2 characters
SSSSS	Serial number	5 digits for serial number, starting from 00001. Reset at start of week to 00001.
Miscellaneous		
ZZ	HW and SW revision	2 alpha-numeric characters
YYYY	Year of manufacturing	4 digits
MM	Month of manufacturing	2 digits
DD	Day of manufacturing	2 digits
COO	Country of origin	E.g. China or Malaysia
	Quick response code	Serial number (MTYYWWXXSSSSS)

3.7 Regulatory Compliance

The transceiver is a Class 1 laser product. It is certified per the following standards:

Feature	Agency	Standard
Laser Eye Safety	FDA/CDRH	CDRH 21 CFR 1040 and Laser Notice 50
Electrical Safety	CB	IEC 60950-1
Electrical Safety	UL/CSA	UL 60950-1 and CAN/CSAN 60950-1

3.8 FCC Class A Notice

Each of the devices complies with CFR47 FCC Class A Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference.
2. This device must accept any interference received, including interference that may cause undesired

Note: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no

guarantee that interference will not occur during installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/television technician for help.

Modifications: Any modifications made to this device that are not approved by NVIDIA may void the authority granted to the user by the FCC to operate this equipment.



4 References

1. SFF-8665: “QSFP+ 28Gb/s 4X Pluggable Transceiver Solution (QSFP28)”, Rev 1.9, June 29, 2015 and associated SFF documents referenced therein:
    a. SFF-8661
    b. SFF-8679
    c. SFF-8662
    d. SFF-8663
    e. SFF-8672
2. IEEE P802.3bs, 200GAUI-4 Interface.
3. InfiniBand HDR IBTA Specification rev 1.4: https://www.infinibandta.org/ibta-specifications-download/
4. Common Management Interface Specification (CMIS) Rev 4.0
5. Directive 2011/65/EU of the European Parliament and of the Council, “on the restriction of the use of certain hazardous substances in electrical and electronic equipment,” July 1, 2011
6. Cable and Transceiver Handling and FAQ - Mellanox/Nvidia Application Note (MLNX-15-3603)
7. Measuring eye Parameters - NVIDIA Application Note (MLNX-15-5400)
8. LinkX® Memory Map – NVIDIA Application Note (MLNX-15-5926).

For more information, please contact your sales representative.

5 Appendix A: Optical Connector and Fiber Cable

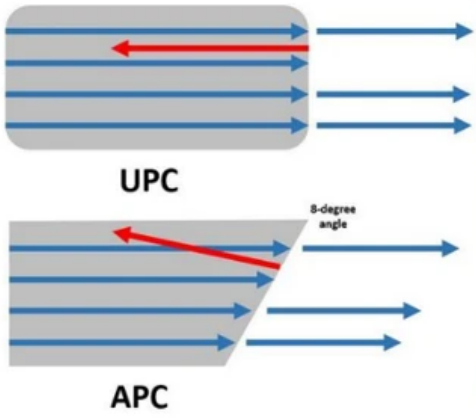
The MPO connectors are the angle-polished (APC) type which provide minimal reflection of the optical signal for optimal signal integrity.

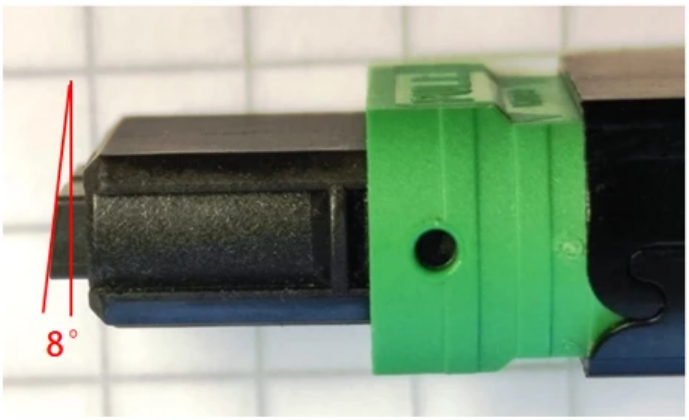
Multimode Fiber Cable with MPO/APC Connectors





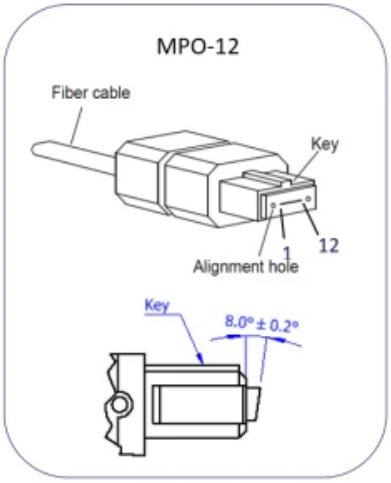
Detail of the MPO/APC Connector



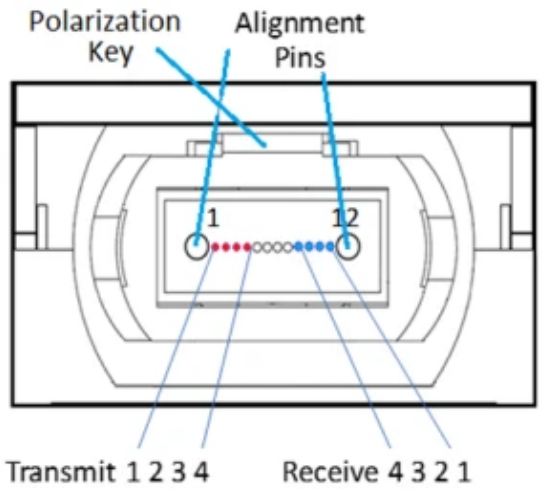


Transceivers have alignment pins for precise positioning of the cable connector against the optical beams. The fiber cable has alignment holes matching the transceiver's pins.

MPO Connector with Alignment Holes and Positioning Key



Optical Receptacle and Lane Assignment (transceiver, front view)



Reference: IEC specification IEC 61754-7.

6 Ordering Information

Legacy OPN	NVIDIA OPN	Description
MMS1V00-WM	980-9I16Y-00W000	Transceiver, 400GbE, QSFP-DD, MPO, 1310nm, DR4

7 Document Revision History

Version	Date	Description of Change
1.5	Aug. 2024	Updated mechanical drawings and front page image.
1.4	Feb. 2023	Updated Appendix A: Optical Connector and Fiber Cable.
1.3	Nov. 2021	Reformatted and rebranded; migrated to HTML.
1.2	Sep. 2021	Updated Applications supported use cases.
1.1	Jul. 2021	Updated Key Features 2km reach information. Updated Operational Specifications table to include both OS1 and OS2 reach information.
1.0	Nov. 2020	First release.

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