



MMS1V70-CM 100GbE QSFP28 DR1 Transceiver Product Specifications

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1 Introduction

NVIDIA® MMS1V70-CM transceiver is a single mode 1-lane (DR1), QSFP28 optical transceiver, designed for use in 100 Gigabit Ethernet (GbE) links on up to 500m of single mode fiber.

The transceiver converts 4 input channels of 25Gb/s NRZ electrical data to a single optical channel of 100Gb/s PAM4 optical signals over a single fiber, using a nominal wavelength of 1310nm, and vice versa for the receive path. The MMS1V70-CM main application is to converge between legacy 100GbE NRZ systems and the emerging 400GbE PAM4 systems. Four different MMS1V70-CM transceivers can be connected to a single 400GbE QSFP-DD MMS1V00-WM DR4 transceiver over a single mode splitter cable.

It is compliant with the QSFP28 MSA, IEEE 802.3bm CAUI-4. Digital diagnostic functions are available via the I2C interface, as specified by the QSFP28 MSA.

Rigorous production testing ensures the best out-of-the-box installation experience, performance, and durability.



Images are for illustration purposes only. Product labels and colors may vary.

1.1 Key Features

- 4x 25Gb/s NRZ Modulation
- Programmable Rx output amplitude and pre-emphasis
- SFF-8665 compliant QSFP56 port
- Single 3.3V power supply
- 4W max power dissipation (typ., each end, with retiming)
- Up to 500m length
- Hot pluggable
- RoHS compliant
- SFF-8636 compliant I2C management interface

1.2 Applications

- Supports 4x MMS1V70-CM on MSN2700 to a single MMS1V00-WM on MSN4700

2 Pin Description

The transceiver's pin assignment is SFF-8679 compliant.

Table 2: QSFP28 Pin Function Definition

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		Vcc Rx	+3.3V Power Supply Receiver	2	2
11	LVC MOS-I/O	SCL	2-wire serial interface clock	3	
12	LVC MOS-I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL	Interrupt	3	
29		Vcc Tx	+3.3V Power supply transmitter	2	2
30		Vcc1	+3.3V Power supply	2	2
31	LVTTL-I	LPMode	Low Power Mode	3	
32		GND	Ground	1	1

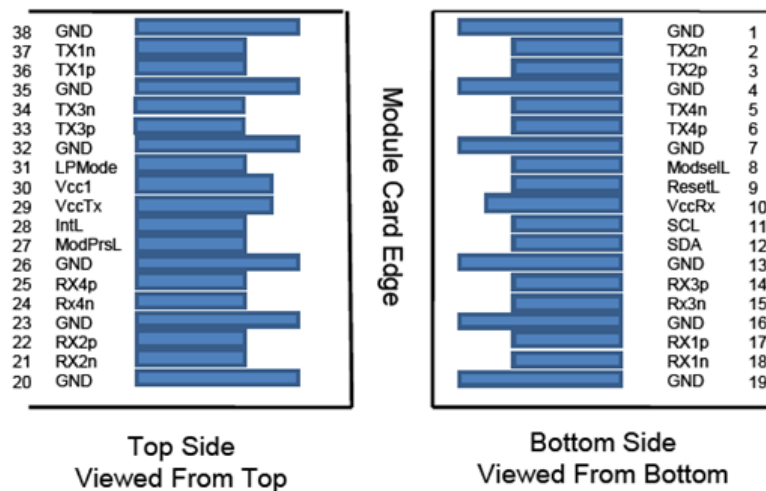
Pin	Logic	Symbol	Description	Plug Sequence	Notes
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1



Notes:

1. GND is the symbol for signal and supply (power) common for the QSFP28 module. All are common within the module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.
2. VccRx, Vcc1 and VccTx are the receiving and transmission power suppliers and shall be applied concurrently. Recommended host board power supply filtering see SFF-8679.

QSFP28 Module Pad Layout:



2.1 Control Signals

The MMS1V70 is SFF-8636 compliant, thus the control signals shown in the pad layout are implemented with the following functions:

Mod PrsL	Output, asserted low	Pull-up by host when no transceiver/cable is present. Connected to ground inside the transceiver. Hence, asserted low when a transceiver/cable is plugged in.
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Mod Sel L	Input, asserted Low	Module Select input pin, terminated high in the module. Only when held low by the host, the module responds to 2-wire serial communication commands. The ModSelL enables multiple modules to share a single 2-wire interface bus.
ResetL	Input, asserted Low	Reset input pin, pulled high in the module. A low level on the ResetL pin for longer than the minimum length initiates a module reset. When de-asserted the transceiver starts its initialization procedure. See the CMIS specification Error! Reference source not found. for details.
LPM ode	Input, asserted high	Low Power Mode input, pulled up inside the module. Hardware control signal for forcing the transceiver into low-power state. Can be overwritten by low-power mode command.
IntL	Output, asserted low	Interrupt Low is an open-collector output, terminated high in the host system. A “Low” indicates a possible module operational fault or a status critical to the host system, e.g. temperature alarm. The host identifies the source of the interrupt using the 2-wire serial interface.

The low-speed signals are Low Voltage TTL (LVTTTL) compliant (except for SCL and SDA signals).

2.2 Diagnostics and Other Features

The transceiver complies with the SFF-8665 specification and has the following key features:

Physical layer link optimization:

- Programmable Tx input equalization
 - Programmable Rx output amplitude
 - Programmable Rx output pre-emphasis
 - Tx/Rx CDR control
- by default enabled for 100 GbE operation, disable it for 40G operation

Digital Diagnostic Monitoring (DDM):

- Rx receive optical power monitor for each lane
- Tx transmit optical power monitor for each lane
- Tx bias current monitor for each lane
- Supply voltage monitor
- Transceiver case temperature monitor
- Warning and Alarm thresholds for each DDM function (not user changeable)

Other SFF-8636 functions and interrupt indications:

- Tx & Rx LOS indication
- Tx & Rx LOL indication
- Tx fault indication

LOS, LOL, and Tx Fault status flags can be read via the two-wire management interface and are jointly transmitted via the IntL output pin. Relevant advertisement, threshold, and readout registers are found in the SFF-8636 MSA.

3 Specifications

3.1 Absolute Maximum Specifications

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module

Parameter	Symbol	Min	Max	Units
Storage Temperature	TS	-40	+85	°C
Supply Voltage	VCC	-0.3	3.6	V
Relative Humidity (non-condensing)	RH	5	95	%
Data Input Voltage - Differential	IVDIP-VDINI	-	1.0	V
Control Input Voltage	VI	-0.3	V _{CC} +0.5	V
Control Output Current	IO	-20	20	mA

3.2 Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Operating Case Temperature	TOPR	0	-	70	°C	
Power Supply Voltage	VCC	3.135	3.3	3.465	V	
Instantaneous peak current at hot plug	ICC_IP	-	-	1600	mA	
Sustained peak current at hot plug	ICC_SP	-	-	1320	mA	
Maximum Power Dissipation	PD	-	-	4	W	1
Maximum Power Dissipation, Low Power Mode	PDLP	-	-	1.5	W	
Signalling Rate	SR	-	53.125	-	GBd	
Control Input Voltage High	V _{IH}	V _{CC} *0.7	-	V _{CC} +0.3	V	
Control Input Voltage Low	V _{IL}	-0.3	-	V _{CC} *0.3	V	
Two Wire Serial Interface Clock Rate	-	-	-	400	kHz	
Power Supply Noise	-	-	-	66	mVpp	10Hz -10MHz
Rx Differential Data Output Load	-	-	100	-	ohms	
Operating Distance	-	2	-	500	m	

Note 1: with power supply voltage 3.3V.

3.3 Optical Specifications

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
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Transmitter						
Wavelength	λ_C	1304.5	1311	1317.5	nm	
Side mode suppression ratio	SMSR	30	-	-	dB	
Average Optical Launch Power	P_{OUT}	-2.9	-	4	dBm	
Average Launch Power Tx_Off	P_{OUT_OFF}	-	-	-15	dBm	
Extinction Ratio	ER	3.5	-	-	dB	
Outer Optical Modulation Amplitude	OMA_{outer}	-0.8	-	4.2	dBm	
Launch Power in OMA_{outer} minus TDECQ for ER ≥ 5 dB	$OMA_{outer} - TDECQ$	-2.2	-	-	dBm	
Launch Power in OMA_{outer} minus TDECQ for ER < 5 dB	$OMA_{outer} - TDECQ$	-1.9	-	-	dBm	
Transmitter and dispersion eye closure	TDECQ	-	-	3.4	dB	
$TDECQ - 10 \log_{10}(C_{eq})$		-	-	3.4	dB	
Transmitter transition time	T_{Tx}	-	-	17	ps	
$RIN_{15.5OMA}$	RIN	-	-	-136	dB/Hz	
Optical return loss tolerance	ORLT	-	-	15.5	dB	
Transmitter reflectance	TR	-	-	-26	dB	
Receiver						
Wavelength	λ_C	1304.5	1311	1317.5	nm	
Damage Threshold		5	-	-	dBm	
Average receive power		-5.9	-	4	dBm	

Receive power (OMA _{outer})	RP	-	-	4.2	dBm	
Receiver reflectance	RR	-	-	-26	dB	
Receiver sensitivity (OMA _{outer})	RS	max(-3.9, SECQ-5.3)	dBm			
Stressed receiver sensitivity	SRS	-	-	-1.9	dBm	
Stressed Receiver Sensitivity Test Conditions:						
Stressed eye closure for PAM4 (SECQ)	SECQ	-	-	3.4	dB	
SECQ-10log ₁₀ (C _{eq})	-	-	-	3.4	dB	

Note: Amplitude customization beyond these specs is dependent on validation in customer system.

3.4 Electrical Specifications

Low-Speed Signal: Compliant to SFF-8679

High-Speed Signal: Compliant to CAUI-4 (IEEE 802.3-2018)

Support for 100GAUI-4 at 26.5625 Gbd when using KP4 FEC

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Transmitter						
LPMode, Reset and ModSelL	V _{IL}	-0.3	-	V _{CC} *0.3	V	
	V _{IH}	V _{CC} *0.7	-	V _{CC} +0.3	V	
Differential Data Input Amplitude	V _{IN,P-P}	95	-	900	mVpp	Note 1
Differential Termination Mismatch		-	-	10	%	
Receiver						
ModPrsL and IntL	V _{OL}	0	-	0.4	V	I _{OL} =4mA
	V _{OH}	V _{CC} -0.5	-	V _{CC} +0.3	V	I _{OL} =-4mA
Differential Data Output Amplitude	V _{OUT,P-P}	250	-	900	mVpp	Note 1

Differential Termination Mismatch		-	-	10	%	
Output Rise/Fall Time, 20%-80%	T _R	9.5	-	-	ps	

Note: Amplitude customization beyond these specs is dependent on validation in customer system.

3.5 Handling and Cleaning

The transceiver can be damaged by exposure to current surges and over voltage events. Take care to restrict exposure to the conditions defined in Absolute Maximum Ratings. Observe normal handling precautions for electrostatic discharge-sensitive devices. The transceiver is shipped with dust caps on both the electrical and the optical port. The cap on the optical port should always be in place when there is no fiber cable connected. The optical connector has a recessed connector surface which is exposed whenever it has no cable nor cap.

Prior to insertion of the fiber cable, clean the cable connector to prevent contamination from it. The dust cap ensures that the optics remain clean and no additional cleaning should be needed. In the event of contamination, standard cleaning tools and methods should be used. Liquids must not be applied.

3.6 Regulatory Compliance

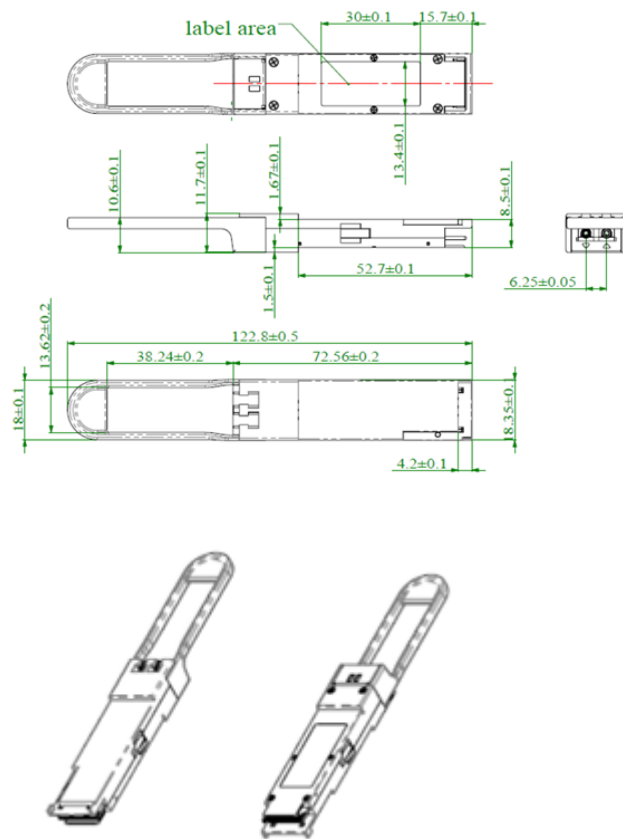
The transceiver is a Class 1 laser product. It is certified per the following standards:

Feature	Agency	Standard
Laser Eye Safety	FDA/CDRH	CDRH 21 CFR 1040 and Laser Notice 50
Electrical Safety	CB	IEC 60950-1
Electrical Safety	UL/CSA	UL 60950-1 and CAN/CSAN 60950-1

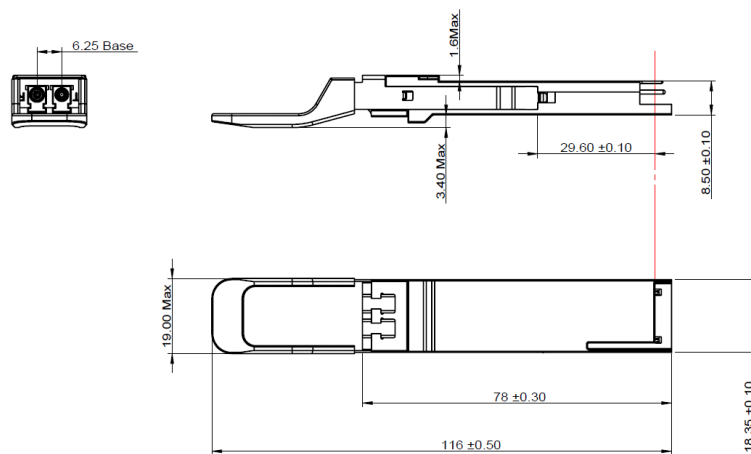
3.7 Mechanical Specifications

Mechanical Dimensions

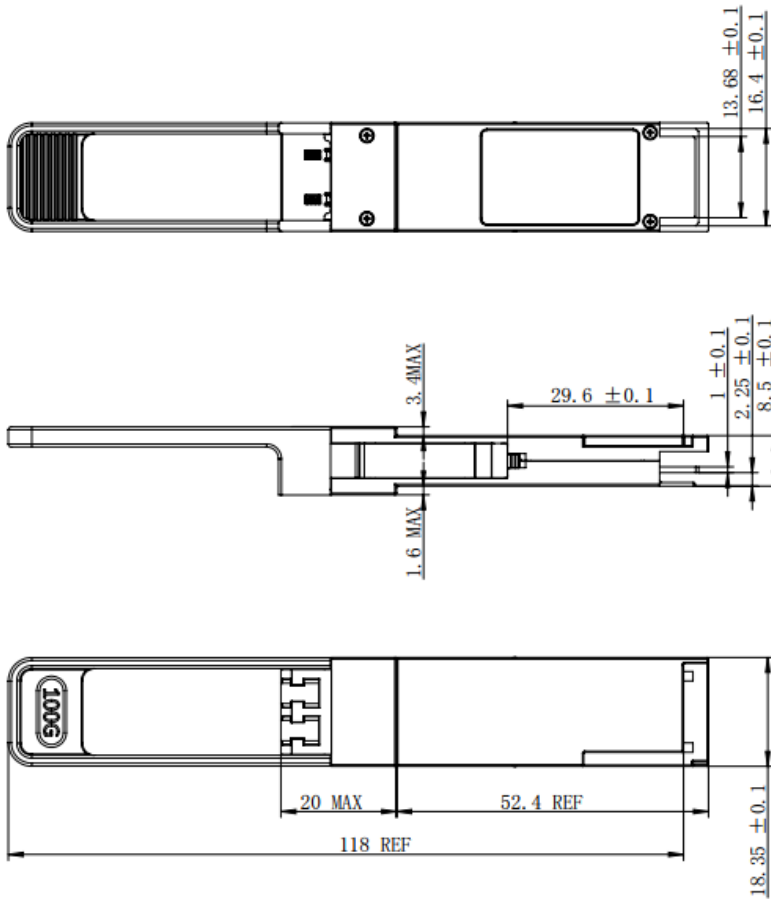
Option 1:



Option 2:



Option 3:

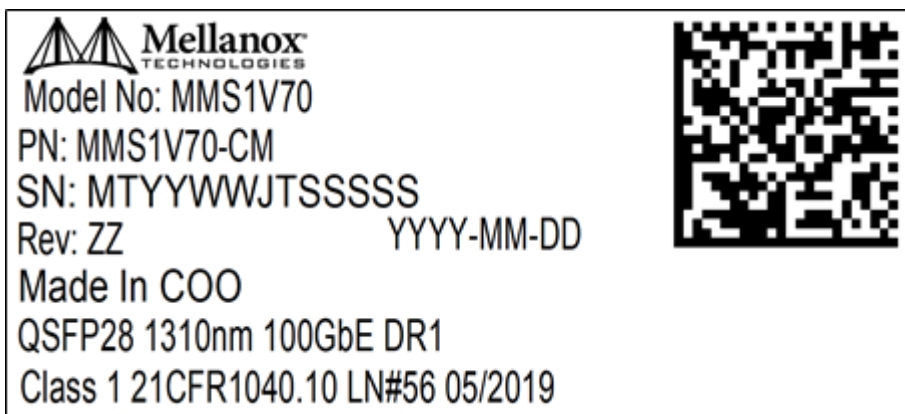


3.8 Memory Map

See LinkX[®] Memory Map Application Note (MLNX-15-5926).

3.9 Label

An example of the label applied on the transceiver's back-shell is illustrated below.





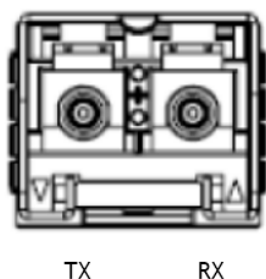
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3.9.1 Transceiver Back-Shell Label Serial Number Legend

Symbol	Meaning	Notes
MT	Manufacturer name (Mellanox/ NVIDIA)	2 digits (alphanumeric)
YY	Year of manufacturing	2 last digits of the year (numeric)
WW	Week of manufacturing	2 digit (numeric)
JT	Manufacturer Site: JT (Taiwan)	Two characters
SSSSS	Serial number	5 digits (decimal numeric) for serial number, starting from 00001.
MM	Month	2 digit (numeric)
DD	Day	2 digit (numeric)
ZZ	Revision Number	2 digits (alphanumeric)

4 Appendix A: Optical Connector and Fiber Cable

The optical port in the transceiver is a pair of LC connectors which mate with fiber-optic cables with duplex LC connector.



Optical LC Receptacle (transceiver, front view)

Reference: IEC specification IEC 61754-20.

The fiber which connects transceiver A's lane 1 must end at transceiver B's lane 2 at the other end of the link. This calls for a crossed cable, also referred to as 'Type B'. The fiber is standard single mode fiber.

Table 8: LC to LC Cable Fiber Connections

Connector A Duplex LC	Connection	Connector B Duplex LC
1	--->	2
2	<---	1

Multiple LC patch cables can be connected in series, but each added connector pair adds reflections and modal dispersion in the link which again impairs performance. An odd number of 'crosses' must be used between transceivers at the two ends.

Typical look of a Single Mode LC Fiber Patch Cable:



Remember to clean the connectors with a fiber cleaner before plugging the cable in.

5 Ordering Information

Part Numbers and Description

Legacy OPN	NVIDIA OPN	Description
MMS1V70-CM	980-9I042-00C000	Mellanox® transceiver, 100GbE, QSFP28, LC-LC, 1310nm, DR1

6 References

- L QSFP Quad Small Form Factor Pluggable - Concept: SFF-8665: <https://www.snia.org/technology-communities/sff/specifications>
- QSFP Quad Small Form Factor Pluggable - Management: SFF-8636: <https://www.snia.org/technology-communities/sff/specifications>
- InfiniBand Architecture Specification and FAQ: <https://www.infinibandta.org/ibta-specification/>
- Environmental and Regulatory compliance statements: <https://www.nvidia.com/en-us/networking/environmental-and-regulatory-compliance/>
- NVIDIA Networking Cable Configurator: <https://www.nvidia.com/en-us/networking/configuration-tools/>

For documentation, please contact your sales representative.

7 Revision History

Version	Date	Description of Change
1.4	Jul. 2026	Added 3rd option mechanical drawings.
1.3	Jul. 2024	Updated mechanical drawings.
1.2	Jun. 2024	Added second option mechanical specifications.
1.1	Jan. 2022	Updated Power Dissipation typo in Key Features section.
1.0	Jul. 2021	First release.

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