NVIDIA MMS1X00-NS400 400Gb/s Single-port QSFP112 Single Mode Transceivers Product Specifications

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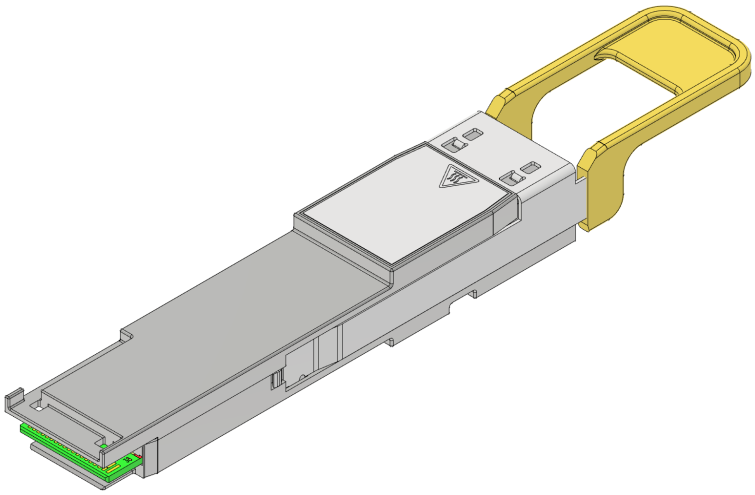
1 Introduction

The NVIDIA MMS1X00-NS400 is an InfiniBand and Ethernet 400Gb/s, Single-port, QSFP112, DR4 single mode parallel transceiver using a single, 4-channel MPO-12/APC optical connector. The Datacenter Reach 4-channel (DR4) design uses 100G-PAM4 modulation and has a maximum fiber reach of 500-meters and assumes two optical patch panels in the link. It has identical design and internals as the OSFP version, only with different connector shells.

The transceiver firmware supports both InfiniBand and Ethernet and is automatically enabled depending on the protocol of the switch attached to. The QSFP112 shell has a flat-top and utilizes the riding heat sink (cooling fins) on the ConnectX-7 or BlueField-3 connector cage. The surface near the pull tab provides additional cooling and remains outside the host connector cage.

Single mode optics is denoted by a yellow-colored pull tab and optical fiber. Green plastic shell on the MPO-12/APC optical connector denotes Angled Polish Connector (APC) and is not compatible with the aqua colored Ultra-flat Polished Connectors (UPC).

NVIDIA's Single-port and Twin-port transceiver combinations guarantee optimal operation in NVIDIA end-to-end InfiniBand systems and a rigorous production tested to ensure the best out-of-the-box installation experience, performance, and durability.



Images are for illustration purposes only. Product labels, colors, and lengths may vary.

1.1 Key Features

- IB and ETH support
- 400G DR4 single mode transceiver
- 4-channels of 100G-PAM4 electrical and optical modulation
- QSFP112 connector shell
- 1310nm EML single mode laser
- Single MPO-12/APC optical connector
- 500m max reach
- 9.5W max (4-channels)

- Single 3.3V power supply
- Class 1 laser safety
- Hot pluggable, RoHS compliant
- Adaptive Tx input equalizer
- QSFP112 MSA
- CMIS 4.0 compliant
- Case temperature range of 0°C to +70°C

1.2 Applications

- Used in ConnectX-7/QSFP112 adapters or BlueField-3/QSFP112 DPUs linked to Twin-port transceivers in 2x400G IB/EN switches

2 Overview

2.1 Transceiver Connectivity Scenarios

The transceiver is used for connecting 400G and 200Gb/s BlueField-3/QSFP112 Data Processing Units (DPU) or 200Gb/s ConnectX-7/QSFP112-based Host Channel Adapter (HCA) PCIe-based network cards. Typically, the transceiver is linked to a single 800Gb/s Twin-port 2x400G OSFP transceiver (MMS4X00-NS) in a Quantum-2 InfiniBand or Spectrum-4 Ethernet switch.

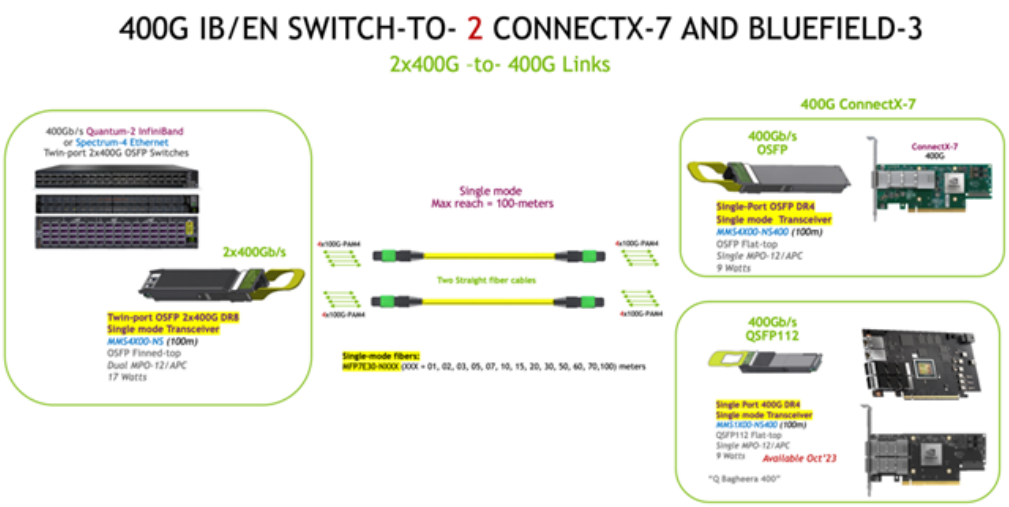
400Gb/s mode: Using 4-channels and straight 500-meter crossover fiber cables (MFP7E30), the transceiver draws 9 Watts maximum or 9 Watts typical. In this case, the Twin-port 2x400G transceiver supports 400G transceivers in two ConnectX-7/QSFP112 and/or two BlueField-3/QSP112 DPU cards.

- QSFP112 ports are not for use in switches. BlueField-3 only accepts QSFP112 ports.
- Both fibers in the Twin-port 2x400G transceiver linked to the QSFP112s must be the same type.

2.2 Use Cases

Switch-to-two 400G ConnectX-7/QSFP112 or BlueField-3/QSFP112
A Twin port QSFP transceiver using two, straight fiber cables can support up to two ConnectX-7 adapters and/or two BlueField-3/QSFP112 DPUs. Each of the two, 4-channel fiber cables (MFP7E30) can link to the 400G QSFP112 MMS1X00-NS400 transceiver up to 100-meters.

- ConnectX-7 adapters are offered on both OSFP and QSFP112
- BlueField-3 Platforms only accept QSFP112 devices

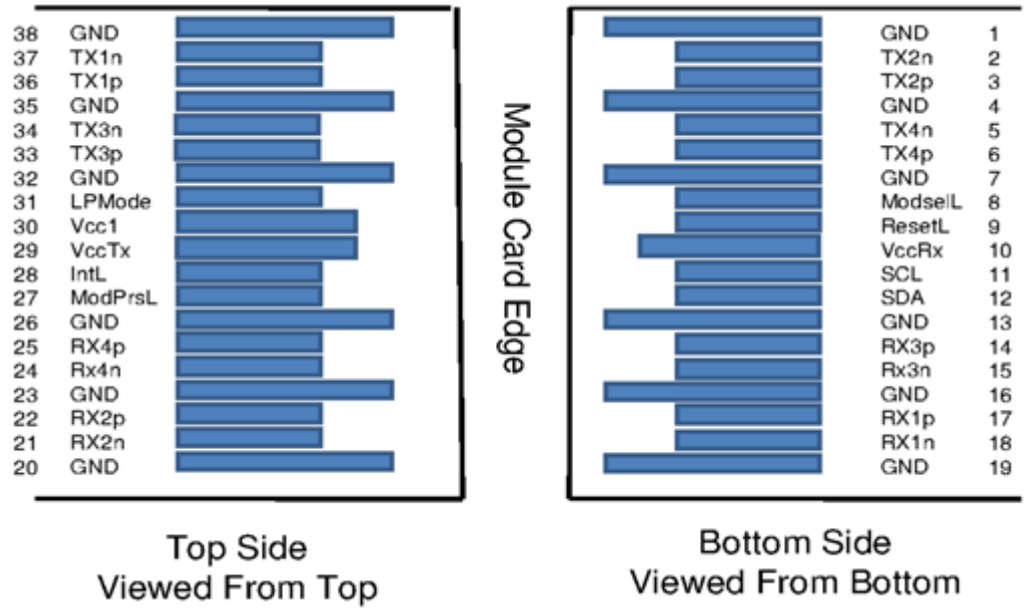


3 Pin Description

3.1 QSFP112 Pin Description

Pin	Symbol	Description	Pin	Symbol	Description
1	GND	Ground	20	GND	Ground
2	Tx2n	Transmitter Inverted Data Input	21	Rx2n	Receiver Inverted Data Output
3	Tx2p	Transmitter Non-Inverted Data Input	22	Rx2p	Receiver Non-Inverted Data Output
4	GND	Ground	23	GND	Ground
5	Tx4n	Transmitter Inverted Data Input	24	Rx4n	Receiver Inverted Data Output
6	Tx4p	Transmitter Non-Inverted Data Input	25	Rx4p	Receiver Non-Inverted Data Output
7	GND	Ground	26	GND	Ground
8	ModSelL	Module Select	27	ModPrsL	Module Present
9	ResetL	Module Reset	28	IntL	Interrupt
10	Vcc Rx	+3.3V Power Supply Receiver	29	Vcc Tx	+3.3V Power Supply Transmitter
11	SCL	2-wire Serial Interface Clock	30	Vcc1	+3.3V Power Supply
12	SDA	2-wire Serial Interface Data	31	LPMode	Low Power Mode
13	GND	GND	32	GND	Ground
14	Rx3p	Receiver Non-Inverted Data Output	33	Tx3p	Transmitter Non-Inverted Data Input
15	Rx3n	Receiver Inverted Data Output	34	Tx3n	Transmitter Inverted Data Input
16	GND	Ground	35	GND	Ground
17	Rx1p	Receiver Non-Inverted Data Output	36	Tx1p	Transmitter Non-Inverted Data Input
18	Rx1n	Receiver Inverted Data Output	37	Tx1n	Transmitter Inverted Data Input
19	GND	Ground	38	GND	Ground

3.1.1 Pin *definitions* of the module high speed inputs/ outputs:



3.2 Control Signals

This transceiver is CMIS 4.0 compliant. This means that the control signals shown in the pad layout support the following functions:

Name	Description
ModPrsL	Module Present pin, grounded inside the module. Terminated with pull-up in the host system. Asserted low when the transceiver is inserted, whereby the host detects the presence of the transceiver.
ModSelL	Module Select input pin, terminated high in the module. Only when held low by the host, the module responds to 2-wire serial communication commands. The ModSelL enables multiple modules to share a single 2-wire interface bus.
ResetL	Reset input pin, pulled high in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. During reset the host shall disregard all status bits until the module indicates completion of the reset interrupt by asserting IntL signal low with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module completes the reset interrupt without requiring a reset.
LPMode	Low Power Mode input, pulled up inside the module. The transceiver starts up in low-power mode, i.e. <1.5 W with the two-wire interface active. The host system can read the power class declaration from the transceiver and determine if it has enough power to enable the high-speed operation/high power mode of the transceiver. This can be done by asserting LPMode low or by use of the Power_over-ride and Power_set control bits (Address A0h, byte 93 bits 0,1).

IntL	Interrupt Low is an open-collector output, terminated high in the host system. A “Low” indicates a possible module operational fault or a status critical to the host system, e.g. temperature alarm. The host identifies the source of the interrupt using the 2-wire serial interface. The INTL pin is de-asserted “High” after completion of reset, when byte 2 bit 0 (Data Not Ready) is read with a value of ‘0’.

3.3 Diagnostics and Other Features

The transceiver supports the QSFP112 MSA specification and has the following key features:

Physical layer link optimization:

- Programmable Tx input equalization
- Programmable Rx output amplitude
- Programmable Rx output pre-emphasis

Digital Diagnostic Monitoring (DDM):

- Rx receive optical power monitor for each lane
- Tx transmit optical power monitor for each lane
- Tx bias current monitor for each lane
- Supply voltage monitor
- Transceiver case temperature monitor
- Warning and Alarm thresholds for each DDM function (not user changeable)

Other SFF-8636 functions and interrupt indications:

- Tx & Rx LOS indication
- Tx & Rx LOL indication
- Tx fault indication

LOS, LOL, and Tx Fault status flags can be read via the two-wire management interface and are jointly transmitted via the IntL output pin. Relevant advertisement, threshold, and readout registers are found in the SFF-8636 MSA.

4 Specifications

4.1 Absolute Maximum Specifications

Absolute maximum ratings are those beyond which damage to the device may occur.

Prolonged operation between the operational specifications and absolute maximum ratings is not intended and may cause permanent device degradation.

Parameter	Symbol	Min	Max	Units
Storage Temperature	T_S	-40	85	°C
Operating Case Temperature	T_{OP}	0	70	°C
Supply Voltage	Vcc	-0.5	3.6	V
Relative Humidity (non-condensing)	RH – Option 1	0	85	%

4.2 Recommended Operating Conditions and Power Supply Requirements

Parameter	Symbol	Min	Typ	Max	Units
Power Supply Voltage	VCC	3.135	3.3	3.465	V
Instantaneous peak current at hot plug (400G)	ICC_IP	-	-	-	mA
Sustained peak current at hot plug (400G)	ICC_SP	-	-	-	mA
Maximum Power consumption (400G)	PD	7	8	9.5	W
Maximum Power consumption, Low Power Mode (400G)	PDLP	0.16	0.18	0.25	W
Instantaneous peak current at hot plug (200G)	ICC_IP	-	-	-	mA
Sustained peak current at hot plug (200G)	ICC_SP	-	-	-	mA
Maximum Power consumption (200G)	PD	-	-	-	W
Maximum Power consumption, Low Power Mode (200G)	PDLP	-	-	-	W
Signaling Rate per Lane	SRL	-	53.125	-	GBd
Two Wire Serial Interface Clock Rate	-	100	400	1000	kHz
Power Supply Noise Tolerance (10Hz - 10MHz)	-	-	-	66	mV
Rx Differential Data Output Load	-	80	100	120	Ohm
Operating Distance	-	-	-	500	m

4.3 Electrical Specifications

Parameter	Min	Typ	Max	Units
Receiver (Module Input)				

AC common-mode output Voltage (RMS)	0	12	32	mV
Differential output Voltage (Long mode)	690	730	770	mV
Differential output Voltage (Short mode)	510	550	590	mV
Near-end Eye height, differential	35	50	65	mV
Far-end Eye height, differential	15	25	35	mV
Far end pre-cursor ratio	-4.5	-	2.5	%
Differential Termination Mismatch	0	1.5	3	%
Transition Time (min, 20% to 80%)	8.5	12	16	ps
DC common mode Voltage	60	-30	0	mV
Transmitter (Module Input)				
Differential pk-pk input Voltage tolerance	750	-	-	mV
Differential termination mismatch	-	-	10	%
Single-ended voltage tolerance range	-0.4	-	3.3	V
DC common mode Voltage	-350	-	2850	mV

Notes:

Amplitude customization beyond these specs is dependent on validation in customer system.

4.3.1 Electrical Specification for Low Speed Signal

Parameter	Symbol	Min	Max	Units
Module output SCL and SDA	VOL	0	0.4	V
	VOH	VCC-0.5	VCC+0.3	V
Module Input SCL and SDA	VIL	-0.3	VCC*0.3	V
	VIH	VCC*0.7	VCC+0.5	V

4.4 Optical Specifications

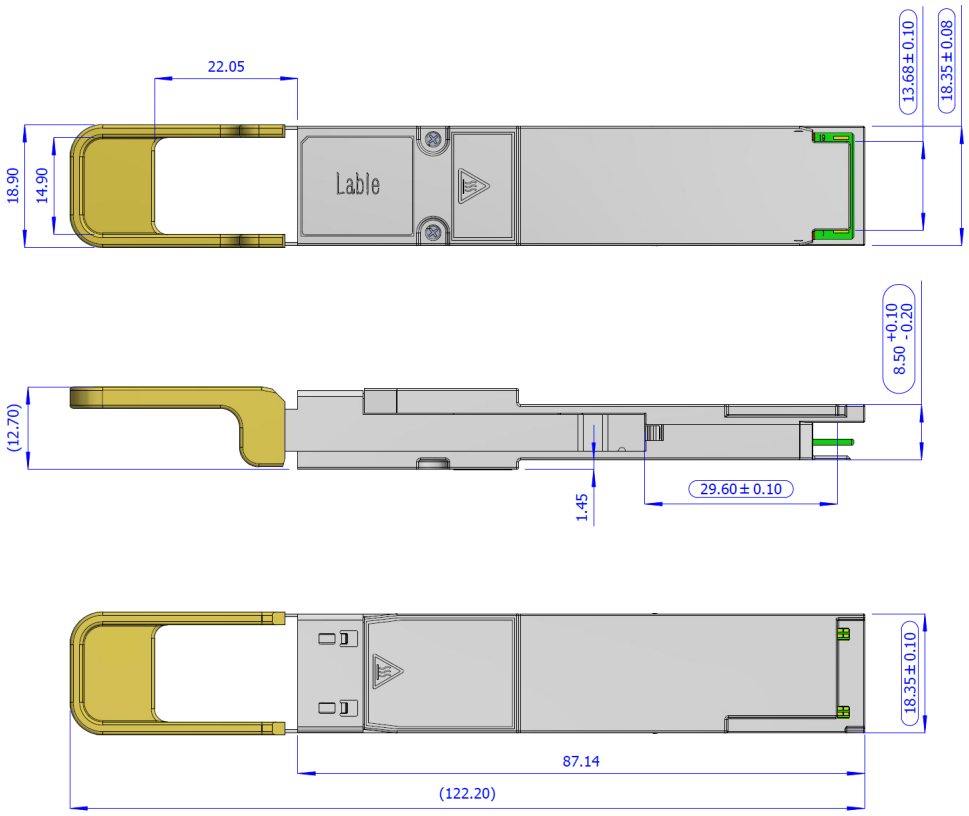
Parameter	Symbol	Min	Typ	Max	Unit	Notes
Transmitter						
Wavelength	λC	1306	1310	1315	nm	
Side Mode Suppression Ratio	SMSR	53	57	61	dB	
Average Launch Power, each lane	AOPL	0.5	2.0	3.5	dBm	1
Outer Optical Modulation Amplitude (OMAouter), each lane	TOMA	0.5	2.0	3.5	dBm	2
Launch Power in OMAouter minus TDECQ, each lane	TOMA-TDECQ	-1.0	0.5	2.0	dBm	

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each lane	TDECQ	0.5	1.0	1.5	dB	
Average Launch Power of OFF Transmitter, each lane	TOFF	-40	-30	-15	dBm	
Extinction Ratio, each lane	ER	4.2	4.7	5.2	dB	
RIN21.4OMA	RIN	-147	-144	-140	dB/Hz	
Optical Return Loss Tolerance	ORL	-	-	15	dB	
Transmitter Reflectance	TR	-28	-24	-20	dB	3
Receiver						
Wavelength	λC	1304.5	1310.5	1317.5	nm	
Damage Threshold, each lane	AOPD	5	5	5	dBm	
Average Receive Power, each lane	AOPR	-	-	4.5	dBm	
Receive Power (OMAouter), each lane	OMA-R	-	-	5.5	dBm	
Receiver Reflectance	RR	-40	-35	-31	dB	
Stressed Receiver Sensitivity (OMAouter), each lane	SOMA	-8.5	-7	-5.5	dBm	4
Receiver Sensitivity (OMAouter), each lane	SRS	-9.3	-8	-6.5	dBm	5
Conditions of stressed receiver sensitivity test						
Stressed eye closure for PAM4 (SECQ)			3.4		dB	
OMAouter of each aggressor lane			4.2		dBm	

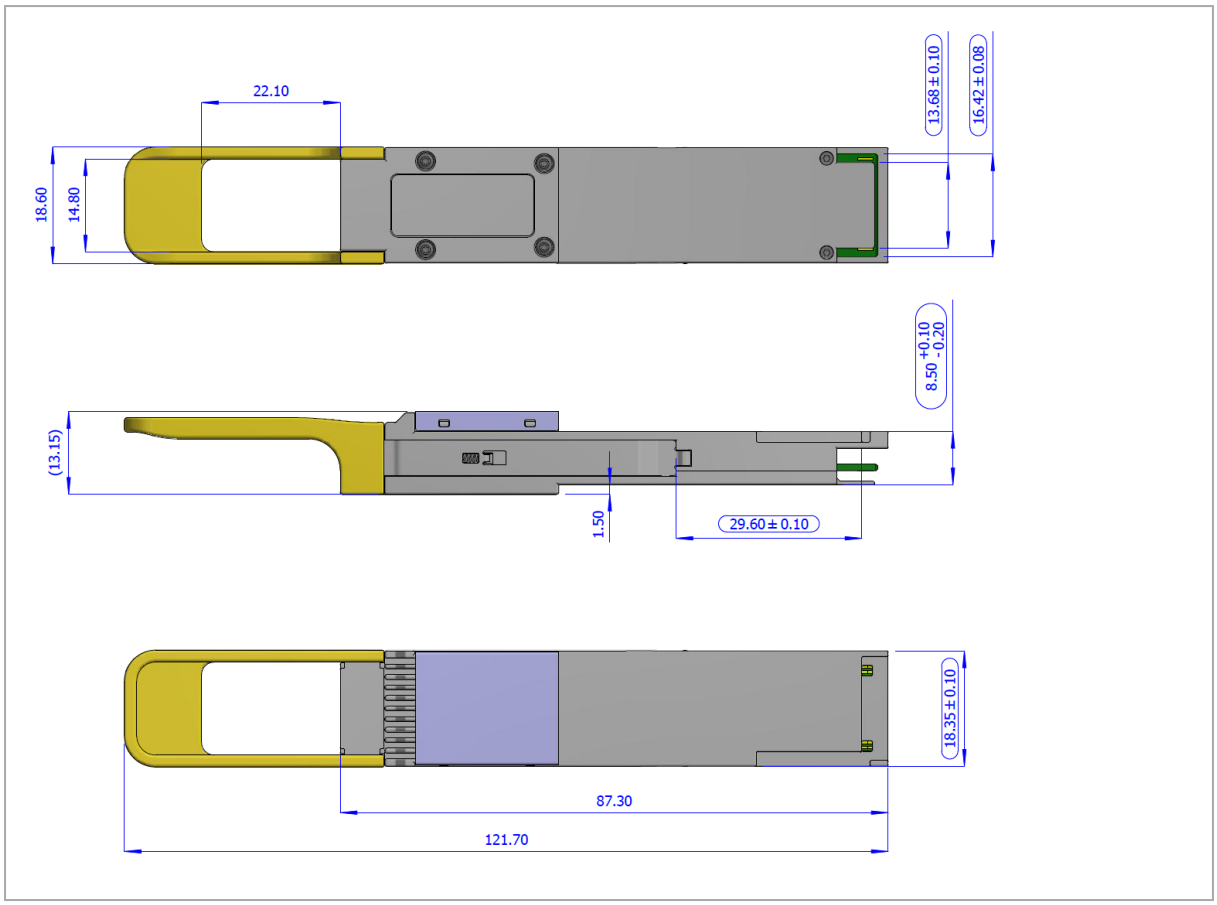
Notes:
1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength.
2. Even if TDECQ < 1.4dB, OMAouter (min) must exceed this value.
3. Transmitter reflectance is defined looking into the transmitter.
4. Receiver sensitivity (OMAouter), each lane (max) is informative and is defined for a transmitter with SECQ of 0.9 dB.
5. Measured with conformance test signal at TP3 for the BER = 2.4x10-4

4.5 Mechanical Specifications

Source 1


22.05
18.90
14.90
Lable
13.68±0.10
18.35±0.08
8.50 +0.10 -0.20
(12.70)
29.60±0.10
1.45
18.35±0.10
87.14
(122.20)

Source 2



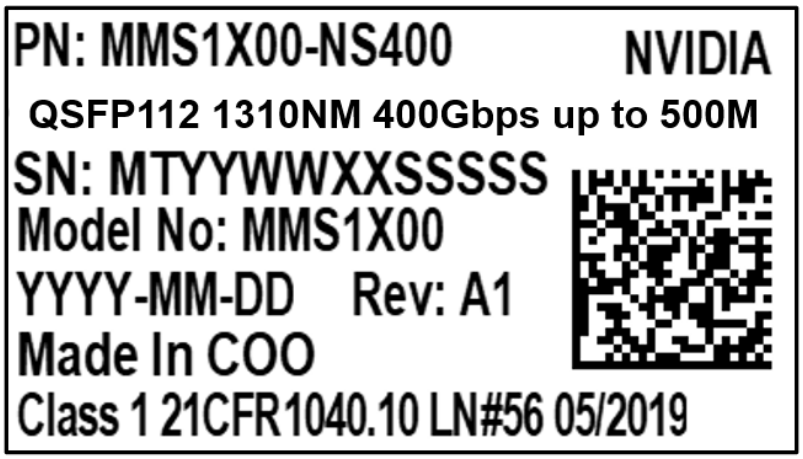
Images are for illustration purposes only. Product labels, colors, and form may vary.

4.6 Labels

4.6.1 Back-Shell Label

The label applied on the transceiver's back-shell is illustrated below. Note that the Images are for illustration purposes only. Labels look and placement may vary.

Transceiver Label (Illustration)



Images are for illustration purposes only. Product labels, colors, and form may vary.

4.6.1.1 Transceiver Back-Shell Label Serial Number Legend

Symbol	Meaning	Notes
MT	Manufacturer name	2 digits (alphanumeric)
YY	Year of manufacturing	2 last digits of the year (numeric)
WW	Week of manufacturing	2 digits (numeric)
NS	Manufacturer Site: China	Two characters
SSSSS	Serial number	5 digits (decimal numeric) for serial number, starting from 00001.

4.6.2 Regulatory Compliance

The transceiver is a Class 1 laser product. It is certified per the following standards:

Feature	Agency	Standard
Laser Eye Safety	FDA/CDRH	CDRH 21 CFR 1040 and Laser Notice 50
Electrical Safety	CB	IEC 62368
Electrical Safety	UL/CSA	UL 62368 and CAN/CSAN 62368

4.7 Connector and Cabling Details

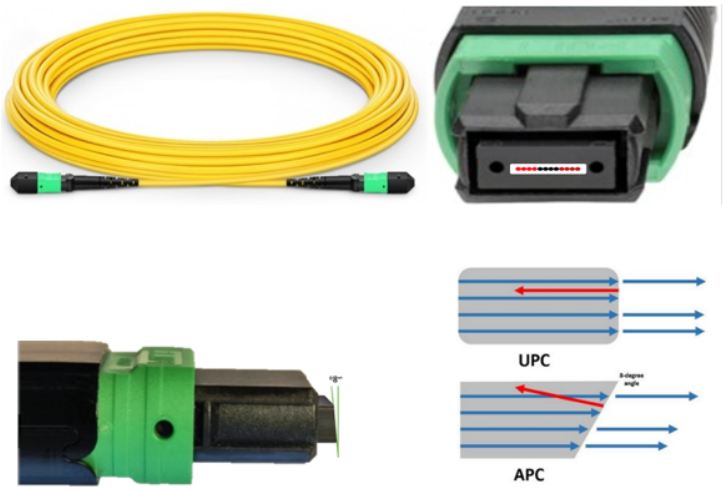
4.7.1 MPO-12/APC Optical Connector

The Twin-port NDR transceiver has a unique NVIDIA patented design enabling two, multiple-push-on/angled-polished-connector 12-fiber (MPO-12/APC) optical connectors per single OSFP form-factor by turning the optical connectors vertically in the twin-port transceiver end. This enables it to host two NDR transceivers inside, each with its own MPO-12/APC optical connector operating independently that can link to another Twin-port transceiver or to a single-port 400Gb/s NDR transceiver.
The MPO-12 has a 12-fiber ribbon but only 8-fibers are used – four transmit and four receive fibers for the 4-channels 100G-PAM4.

- The APC design minimizes back reflections and signal interference by diverting back reflected light from the fiber face to be absorbed into the fiber cladding.
- A positioning key on top of the connector together with the alignment pins define the fiber position numbering scheme to align pin 1 in the optical connector to pin 1 in the transceiver also called “polarity”
- Transceivers have alignment pins for precise positioning of the cable connector against the optical beams. The fiber cable has alignment holes matching the transceiver’s pins.
- Important to note that transceivers have pins. Optical connectors have holes used with transceivers have holes. Optical connectors with pins are not compatible with transceivers and used in trunk cabling to connect two fiber cables together.

The MPO-12/APC optical connector is used in both the 100G-PAM4 based single mode and multimode fiber cables.
Single mode optics is denoted by a yellow-colored pull tab and yellow-colored optical fiber. Green plastic shell on the MPO-12/APC connector denotes Angled Polish Connector and is not compatible with Ultra-flat Polished Connectors (UPC) used with slower line rate transceivers.

MPO-12/APC Showing 4-Transmit and 4-Receive Fibers and Angled Polish Connector End Face

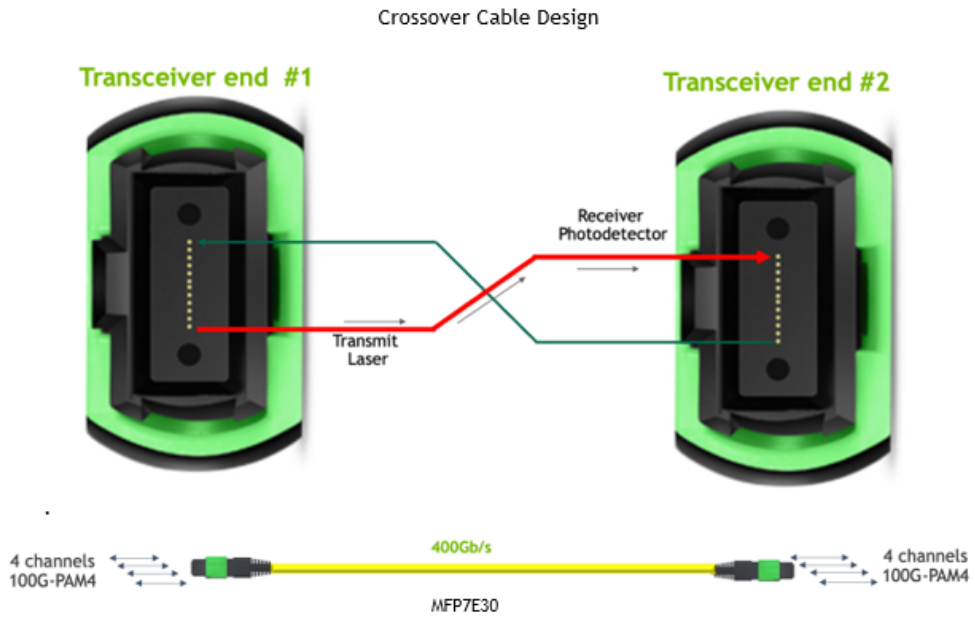


4.7.1.1 NVIDIA Supplied Crossover Type-B Fiber Cables

Linking two transceivers directly together requires aligning the transceiver laser sources with the correct photo detectors in the receive transceiver. Transmit and receive fibers are switched inside the cable enabling two transceivers to be directly connected to each other. This is called a Type-B crossover fiber.

Each of the two 4-channel NDR ports in the Twin-port transceiver has its own 4-channel optical cable that can link to two single-port 400Gb/s transceiver. Two fiber cables are needed for each Twin-port transceiver. Fiber cables are crossover cable Type-B that aligns the transmit laser with the opposite transceiver's receiver photodetector allowing to directly connect two transceivers together to maintain minimum optical losses, lowest back reflections, longest reach and increased reliability without the use of optical patch panels.

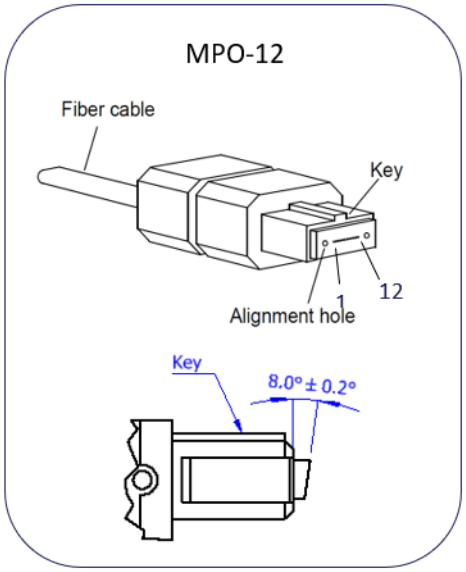
NVIDIA supplies crossover, single mode fiber cables up to 100-meters. For length from 100-to-500-meters, a crossover fiber segment must be implemented in the link to align transmit lasers with receiver photodetectors. This can be implemented by building the fiber cable as a crossover cable, or adding a NVIDIA crossover cable in the link, or via an optical patch panel with a crossover segment.

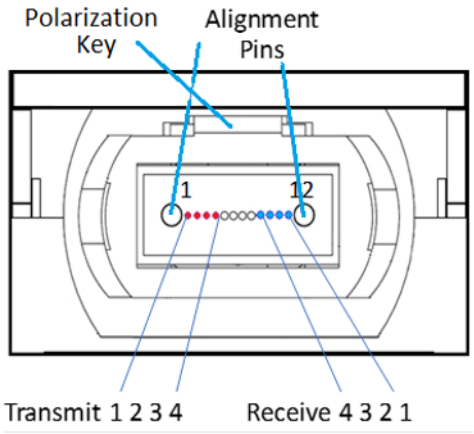


Note: Refer to the Recommended Fiber Cables table for more information.

Transceivers have alignment pins for precise positioning of the cable connector against the optical beams. The fiber cable has alignment holes matching the transceiver's pins.

MPO Connector with Alignment Holes and Positioning Key





NDR transceiver: MPO Receptacle, Lane Assignment, and Positioning Key (front view)

Reference: IEC specification IEC 61754-7

4.7.2 Handling and Cleaning

The transceiver can be damaged by exposure to current surges and over voltage events. Take care to restrict exposure to the conditions defined in Absolute Maximum Ratings. Observe normal handling precautions for electrostatic discharge-sensitive devices.

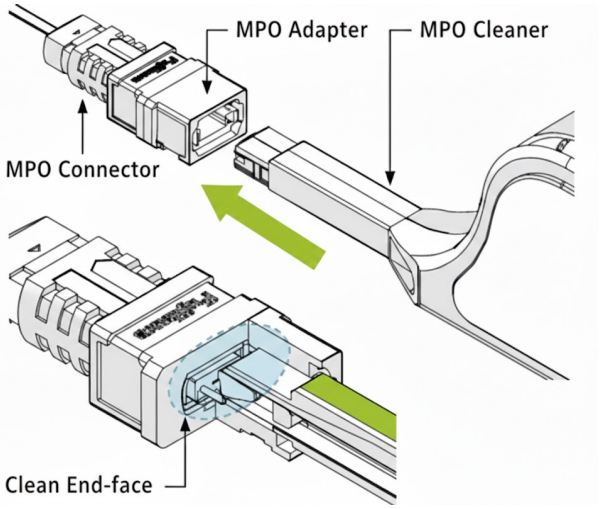
The transceiver is shipped with dust caps on both the electrical and the optical port. The cap on the optical port should always be in place when there is no fiber cable connected. The optical connector has a recessed connector surface which is exposed whenever it has no cable nor cap.

⚠ Important Notes:

1. Keep both the fiber and transceiver dust caps.

2. Clean both transceiver receptacle and cable connector prior to insertion of the fiber cable, to prevent contamination from it. The dust cap ensures that the optics remain clean during transportation. Standard cleaning tools and methods should be used during installation and service. Liquids must not be applied.
3. 80% of transceiver link problems are related to dirty optical connectors.





4.7.3 Cable Management Guidelines

For more information and general interconnect management and installation, see NVIDIA Cable Management Guidelines and FAQ Application Note.

5 Ordering Information

5.1 Part Numbers and Description

Legacy OPN	NVIDIA OPN	Description
MMS1X00-NS400	980-9I068-00NM00	NVIDIA single port transceiver, 400Gbps, NDR, QSFP112, MPO, 1310nm SMF, up to 100m, flat top

6 Recommended NVIDIA Supplied Crossover Fiber Cables Part Numbers



Single-mode, Straight Crossover Fibers

OPN	4-channel MPO/APC to 4-channel MPO/APC
MFP7E30-N003	3m
MFP7E30-N005	5m
MFP7E30-N007	7m
MFP7E30-N010	10m
MFP7E30-N015	15m
MFP7E30-N020	20m
MFP7E30-N030	30m
MFP7E30-N050	50m
MFP7E30-N060	60m
MFP7E30-N070	70m
MFP7E30-N100	100m

7 Document Revision History

Rev	Date	Description
1.4	Nov. 2026	Updated the Optical Specifications table with the correct Receiver sensitivity values.
1.3	Jan. 2026	Updated the Mechanical Specifications section.
1.2	Apr. 2025	Updated the following sections: • Introduction • Overview • Specifications • Recommended NVIDIA Supplied Crossover Fiber Cables
1.1	Apr. 2023	• Updated the document for Ethernet support. • Minor text edits
1.0	Dec. 2022	Initial release.

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